

SE 2450

Frequency Response Analyser



Instruction Manual

EMI SELabs

MS 50093



SE Labs

Instruction Manual

FREQUENCY RESPONSE ANALYSER

SE 2450

MS 50093

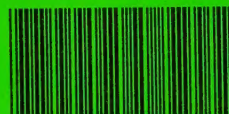
Issue 3

March 1981

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HISTORY SHEET

MANUAL ISSUE	TEXT	CIRCUIT/LAYOUT DIAGRAMS	REMARKS
1			JANUARY 1980 Sections 1 to 4 only.
2			JUNE 1980 Sections 5 to 9 added.
3	Sections 1,2,3,4, 5,6 & 9 revised	Section 8 revised	MARCH 1981 References to options manuals included.



Technical Bulletin

Equipment Type Number: FREQUENCY RESPONSE ANALYSER SE 2450
- INSTRUCTION MANUAL

Modification(s)

C/N No(s)

1. PURPOSE

The purpose of this bulletin is to:

- (a) provide an Appendix to Section 5 of the manual, informing the reader of the various versions of software in existence and to identify the differing features,
- (b) to provide a fault diagnosis procedure (down to board level) to be added to Section 7 of the manual,
- (c) to acquaint the reader with the latest design changes since the Issue 3 was produced.

2. NEW PAGES

Insert Appendix 1 to Section 5 Software Features, immediately after Chapter 5.3 of Section 5, THE FRA SYSTEM.

Insert 5. Fault Diagnosis immediately after page 7.2 of Section 7 TESTING.

Hand Amendments:

SECTION	PAGE	ACTION
5	5.1	Add to List of Contents: 'Appendix A to Section 5. Software Features (SE2461-SE2462)'
7	7.1	Add to List of Contents: '5. Fault Diagnosis'



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3. DESIGN CHANGES

Memory 2 Board (E90917, D82021/02, PL82021/02)

9789: In order to accommodate the new SE 2462 software, it has been necessary to replace the Mitsubishi 2716K PROMS with Mitsubishi 2732K PROMS in IC positions 8C,10C,11C,13C,15C,16C,17C and 18C.
Note: ICs 5C and 7C are no longer used.

IC13D is now programmed to drawing No.C91639.

IC15D is now programmed to drawing No.C91638.

Link LK1 is now linked in position A to C.

On PL82021/02, ICs 1A to 16A and 1B to 16B can be alternatively replaced by Texas TMS 4027-20NL, Stk No.BS6155.

Circuit Diagram E90917 raised to Issue 3.

Assembly Diagram D82021/02 raised to Issue 3.

Parts List 82021/02 raised to Issue 5.

Processor and Cursor Control Board (D802026,PL82026)

9883: To prevent capacitor C3 shorting in the card frame, C3 has been changed to:

Stk No.CS33027, Ceramic trimmer, 2-10pF, CD5/10.

C13 outline changed on Assembly Diagram D82026 (fig 8.3).

Assembly Diagram D82026 raised to Issue 7

Parts List 82036 raised to Issue 17.

9832 Texas IC Type No. changes:

Memory 2 Board (E90917, PL82021/02)

On PL82021/02, items 71 and 72 (ICs 13D and 15D) are now made from Texas TBP 18S030N (Stk No.BS6191). This change also applies to circuit diagram E90917 (Fig 8.5) - see C/N 9789 above.

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9832 Keyboard Control Logic 1 Board (E82085, PL82086)

(contd)

On PL82086, items 88 and 89 (ICs 5A and 5B) are now made from Texas TBP 18S030N (Stk No. BS6191). This change also applied to circuit diagram E82085 (Fig 8.20).

Circuit Diagram E90917 raised to Issue 4.

Parts List 82021/02 raised to Issue 6.

Circuit Diagram E82085 raised to Issue 8.

Parts List 82086 raised to Issue 13.

Alpha-Numeric Control Board (E90200, D90201, PL90201)

ICs 2C, 12D, 14D, 18D are now made from Texas TBP 18S030N now made from BS6191.

Circuit Diagram E90200 raised to Issue 4.

Assembly Diagram D90201 raised to Issue 4.

Parts List 90201 raised to Issue 6.

Correlator Control Board - Fig 8.10A, 8.11 (E82005, D82006, PL82006)

9782: IC6D changed to Texas SN74S74N, Stk No. BS3537.

9825: ICs 1A, 1D, 2A, 3A, 3D and 4A now mounted on 24-pin IC sockets:
Stk No. BS 5136, Type VS-2-24-110-N-B

Circuit Diagram E82005 raised to Issue 9.

Assembly Diagram D82006 raised to Issue 12.

Parts List 82006 raised to Issue 14.

9894: Link shown incorrectly - should be linked A to B.

To reduce noise on the INT SYNC line, a connection has been added from IC6D, pin 14 to edge connector pin B15 (see also C/N 9896 on this bulletin).



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Modification(s)

C/N No(s)

9870/

9931: To overcome erroneous results being displayed, the following modifications have been made (see also C/N 9869 on this bulletin):

Resistor R1 and Test Point TP1 deleted.
Capacitor C30, 100pF, added between IC3B, pin 8 and 0V.
Capacitor C31, 100pF, added between IC2C, pin 8 and 0V.
Capacitors C22 and C23 changed to 10 μ F Electrolytic.

IC8: Texas type No. changed to TBP 18S22N.
LK1: now linked A to B.

On PL 82006:

Resistor R1 deleted.
Capacitors C30 and C31 added:
Stk.No.CS31733, 100pF, $\pm 2.5\%$, 30V, Suflex HS.
Capacitors C22 and C23 changed to:
Stk.No.CS31744, 10 μ F, $\pm 20\%$, 35V ITT, TAG 10/35.

10022: Test sockets TP4, 5 and 6 deleted from Assembly Diagram D82006.

Circuit Diagram E82005 raised to Issue 10.
Assembly Diagram D82006 raised to Issue 14.
Parts List 82006 raised to Issue 15.

9786: Correlator A/D Board - Fig 8.12 (E82040, D82041, PL82041)

Resistors R44 and R45 changed from
470ohm (Stk No.DS32058) to 330ohm (Stk.No.DS34695)

9824: ICs 7E, 7G, 8G, 10A, 10G and 13E now mounted on 8-pin IC sockets,
Stk.No.BS5600.

9869: To overcome erroneous results being exhibited on the display, the following modifications have been made (see also C/N 89870 on this bulletin):

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Equipment Type Number:

Modification(s)

C/N No(s)

9869 IC3F pin 1 disconnected from IC9G, pins 12 and 13 and reconnected
(contd) to IC11A, pin 11 (reset).

Capacitor C87 connected between gates IC12F/6 and 8, 11F/13,
13D/11 and 0V.

IC13A changed from SN74LS74N to SN74L74N (Stk No.BS 6197)

Alternative to IC10D shown is Burr Brown type ADC 84KG-12.

Board Assembly raised to Mod State G

Circuit Diagram E82040 raised to Issue 8.

Assembly Diagram D82041 raised to Issue 10.

Parts List 82041 raised to Issue 15.

Generator D/A Board - Fig 8.9A (E88662,D82036/01,PL82036/01)

9818: Mod State raised to E.

Capacitors C77 and 78 added, values selected on test from the
following:

C77: Stk No. CS32256, 56pF, 2.5%, 30V, Suflex HS

Stk No. CS31899, 68pF, 5%, 30V, Suflex HS68/5-7/30

C78: Stk No. CS31737, 470pF, 2.5%, 30V, Suflex HS

CS31810, 560pF, 2.5%, 30V, Suflex HS

CS31738, 680pF, 2.5%, 30V, Suflex HS30

9879: To reduce the failure rate of IC9B, it is now mounted on a socket:
Stk.No. BS5014, type US-2-16-110-N-B.

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Modification(s)

C/N No(s)

9886: IC9C changed to TBP18S22N.

The following link table has been added to the circuit and component layout diagrams (Fig 8.8A and 8.9A):

NORMAL

OPERATION

LK1	IN
LK2	OUT
LK3	IN
LK4	OUT
LK5	IN
LK6	A to C IN, A to B OUT
LK7	IN
LK8	OUT
LK9	IN
LK10	OUT
LK11	OUT
LK12	OUT
LK13	OUT
LK14	OUT
LK15	A to B IN, A to C OUT
LK16	OUT

9886 On PL82036/01, IC9C is now listed as being programmed to drawing No.C88477 made from IC type TBP18S22N.

P.C.Board raised to MOD STATE F.

9896: To reduce noise on the INT SYNC line a connection has been added from IC6E, pin 8, to edge connector pin B15 (Fig 8.8A) - see also C/N 9894 on this bulletin.

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Modification(s)

C/N No(s)

9974: Note added to circuit diagram E88662 and assembly diagram D82036/01 as follows:

Link LK15 only fitted when SE 2462 software is used. Positions as follows:

LK15A to B for STOP IMMEDIATE

LK15A to C for STOP 0 °

Circuit diagram E88662 raised to Issue 7.
Assembly diagram D82036/01 raised to Issue 8.
Parts Lists 82036/01 raised to Issue 7.

9878: Generator Control Board (D82001, PL82001)

REG1 is now mounted on a pad, Stk.No.BS2263, Jermyn Pad T05-001.

Assembly Diagram D82001 raised to Issue 10.
Parts List raised to Issue 11.

9887: Alpha-Numeric Control Board (E90220, D90221, PL90221)

The following links table has been added to the circuit and component layout diagrams Figs 8.17A and B:

For Alpha-Numeric Display

For Alpha-Numeric and Graphics Display

LK1	IN
LK2	OUT
LK3	OUT
LK4	OUT

LK1	OUT
LK2	IN
LK3	IN
LK4	IN

IC4C on assembly diagram changed to read SN74LS20.



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Modification(s)

C/N No(s)

9887 Item 66 type change to Open Market, Stk. No.BS5064, SN74LS157N.
(contd):

Circuit diagram E90220 raised to Issue 3.
Assembly diagram D90221 raised to Issue 3.
Parts List 90221 raised to Issue 3.

Display Monitor Module

9829. From Contract No 403145, the type 18 module is replaced by type 29A: new Circuit Diagram No. D92370, Assembly Diagram D86872/01 and Parts List 86872/01, to be added to the Instruction Manual.

The basic FRA Assembly Alpha-Numeric SE 2450 Parts List 91065/01 modified to include the following major sub-assembly changes:

Item 6: Control Panel PL82709 changed to Control Panel PL82709/01.

Item 15: CRT Pot Board PL86900 deleted.

Item 16: Monitor Module PL86872 changed to Monitor Module PL86872/01.

Item 22: Chassis Plate changed to PL86761/01.

Item 32: LED Cableform Assembly changed to PL88622/01.

Parts List PL91065/01 raised to Issue 3.

Power Supply (E82070,D82071,D82076,PL82071,PL82076)

9952: To stop the interlock circuit from operating due to excessive current being drawn on the +12V supply, capacitor C26 has been removed and replaced by a wire link.

9897/ It has been observed that sometimes the $\pm 30\%$ supply outputs $\pm 20V$
10010 To overcome this tendency, the following potentiometers have been changed:

On P.C.Board No.1, RV1,2,3 and 4 are now 5K,12-turn, Bourne 3262W-502, Stk.No. FS10910.

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Modification(s)

C/N No(s)

On P.C.Board No.2, RV5,6 and 8 are now 5K, 12-turn, Bourne 3262W-502, Stk.No. FS10910.

Circuit Diagram E82070 raised to Issue 7.
Assembly Diagram D82071 raised to Issue 5.
Assembly Diagram D82076 raised to Issue 7.
Parts List 82071 raised to Issue 7.
Parts List 82076 raised to Issue 14.

9971: FRA Motherboard (E82061)

To prevent the motherboard-to-power-supply cableform being fitted incorrectly, jackscrews have been added to PL18.

Assembly Diagram E82061 raised to Issue 12.
Parts List 82061 raised to Issue 14.

Power Supply 1 Assembly (81221/01)

9950: New Power Supply introduced, superceding power supply assembly 81221, referred to as 'Power Supply 1'. It comprises:

PL 81221/01 Power Supply 1 Assembly
PL 82071/01 P.C.Board 1, Type 1
PL 82076/01 P.C.Board 2, Type 1
PL 82081/01 PSU 1 Motherboard

New diagrams to be added to the manual:

Circuit Diagram E92106
Assembly Diagram D82081/01
Assembly Diagram D82071/01
Assembly Diagram D82076/01
Assembly Diagram E81221/01

10030: On PL 82081/01, alternative connector added for SKT 6 and 7, viz., Skt, 20-way, Pye type MHD 20D-N-01-01 ML/M3-1 and 20.

Parts List 82081/01 raised to Issue 2.

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Modification(s)

C/N No(s)

10039: Motherboard Assembly (E82061)
Back Panel Assembly (PL81224)
IEEE 488 Cableform (PL86882)
Peripheral I/F Cableform 1 (PL86883)
Peripheral I/F Cableform 2 (PL86884)
External Sync Cableform 1 (PL86885)

To prevent the above cableforms being plugged-in the wrong way round on the motherboard, polarizing plugs have been fitted to the following sockets:

SKT 27, plug fitted in position 2
SKT 26, plug fitted in position 13
SKT 28, plug fitted in position 13
SKT 25, plug fitted in position 1
SKT 29, plug fitted in position 7

Add note to Fig 8.29 FRA Motherboard E82061:

'The following pins are cut-off flush with the body of connectors as follows:

SKT	PIN
25	1
26	13
27	2
28	13
29	7

Parts List 81224 raised to Issue 10
Parts List 86882 raised to Issue 5
Parts List 86883 raised to Issue 5
Parts List 86884 raised to Issue 3
Parts List 86885 raised to Issue 4
Assembly Diagram E82061 raised to Issue 13

10042: Generator D/A 2 Board (PL82036/01)

Item 54 now shown as Qty 2-off.

PL 82036/01 raised to Issue 10.

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APPENDIX A TO SECTION 5

FEB 1982

SOFTWARE FEATURES

(SE 2461 - SE 2462)

HARDWARE DIFFERENCES

All versions of software are resident on the Memory Board which plugs into position 10 on the motherboard. There are two types of PROMs which can be used on this board. These are:

- (a) 32K PROM type 2732
- (b) 16K PROM type 2716

The 16K PROM version is only suitable for the SE 2461 version of software while the 32K PROM may be used both for SE 2461 and SE 2462 versions. To convert from SE 2461 software to SE 2462 software proceed as follows:

- (a) Memory boards fitted with 16K PROMs should be modified to accept 32K PROMs:

IC Position	Programmed to SE Labs Drawing No.
15D	C 91639
13D	C 91638

Link 1 connects A to C

- (b) Memory boards already fitted with SE 2461 programmed 32K PROMs should be re-programmed as follows:

IC Position	Programmed to SE Labs Drawing No.
18C	A 92553
17C	A 92554
16C	A 92555
15C	A 92556
13C	A 92557
11C	A 92558

SOFTWARE DIFFERENCES

Figure A5.1 to A5.5 show the format of the various pages which are obtained with the new software.

GENERATOR CONTINUOUS/STOP OPTION

This is a new feature which deals with the operation of the generator after it has made a measurement. If selected, the generator continues to generate a signal. If not selected the generator stops either at the position where a measurement is completed, or at zero volts. This option is selected on the generator D/A board, position 13, link 15. Thus, if link 15 A to B is connected, the generator stops where the measurement is completed. If link 15 A to C is connected the generator stops at zero volts. The factory connection is link 15 A to B.

INTEGRATION TIME

This has been introduced in preference to integration cycles which is used in the SE 2461 version. The advantage of integration time is that each measurement in a sweep takes the same time giving the results to the same accuracy. No measurements can be made at less than 100 ms and if the time taken to make a 1 cycle measurement is greater than 100 ms the machine defaults to 1 cycle. Note that the keyboard button is now labelled INT TIME.

240 RESULTS

The SE 2462 software is capable of storing 240 results and this can be divided equally between the two channels if required. The CHANNEL MEAS field selects which channel requires to be measured and CHANNEL DISP selects the required results. Thus, it is possible to measure both channels and to display the results as required.

GRAPH AXES

When plotting phase angle it is sometimes useful to be able to change the axes to $\pm 180^\circ$ scaling. This avoids sharp changes to the 0 to 360° transition which makes the graph look unrepresentative and untidy.

PHASE RESOLUTION

To improve the resolution of the phase measurement, which can be better than 0.1° at low frequencies, an extra digit is available.

IEEE 488 BUS

The status bytes returned by the SE 2450 contain information relating to the convert and plot sequences of the SE 2450. This enables plots to be made on the screen via the bus.

Thus when G7 is selected, the second byte has additional data on the measurement status - refer to SE 2451/00 Supplement, Section 4, page 4.11.

MEASUREMENT STATUS

0	Ready or over-range
1	Pause or under-range
2	Measure
3	Convert
4	Plot
8	Phase reached (after phase stop is set).

AMPL V
0.00000

PHASE 0
0.0000

S1 [] S2 []
FREQUENCY [] HZ
HARMONIC []
GEN. CONTINUOUS [*]
GEN. AMPLITUDE [.001] V RMS
GEN. BIAS [] V
CORRELATOR RANGE AUTO []
CHANNEL A[500]V B[500]V
INTEGRATION TIME [.1] SECONDS
DELAY [.5] SECONDS
CHANNEL A[*] B[] B/A[]
CO-ORDINATES POLAR
READY

FIGURE A5.1

VOLTAGE RMS[*] PK[]
WAVE SHAPE SIN[*] TRI[] SQRC[]
MEASUREMENT ABS[*] RATIO[]
REPEAT MODE []
BIAS REJECT [] AUTO []
CHANNEL AC 01V BC 01V

STATISTICS []
REPETITIONS [10]
PERIPHERAL OPTIONS
EXTERNAL SYNC []
PRINT RESULTS [] DUMP PAGE [3]
XY PLOTTER TYPE [0]

READY

FIGURE A5.2


```

START FREQUENCY [    1] HZ
FINAL FREQUENCY [  100] HZ
HARMONIC          [  1]
GEN. CONTINUOUS   [*]
GEN. AMPLITUDE   [ .001] V RMS
GEN. BIAS        [    0] V
CORRELATOR RANGE   AUTO [ ]
CHANNEL  A[500]V  B[500]V
INTEGRATION TIME [   .1] SECONDS
DELAY            [   .5] SECONDS
INTERVALS        [  20]
INTERVAL MODE LINEAR[*] LOG[ ]
CHANNELS MEAS A[*] B[ ]
CHANNEL DISP A[*] B[ ] B/A[ ]
CO-ORDINATES  POLAR
                READY

```

FIGURE A5.3

```

                                PAGE  1
NO  FREQ  AMPL  PHASE  S1  S2
   HZ      V      0
1
2
3
4
5
6
7
8
9
10
11
12
CHANNEL A      READY

```

FIGURE A5.4

```

GRAPHICS [ ] X-Y PLOTTER [ ]
OVERLAY  [ ]  AUTOSCALE [*]
Y-AXIS  X-AXIS  TYPE  SELECT
REAL    FREQ    CO-QUAD [ ]
IMAG    FREQ    CO-QUAD [ ]
GAIN    FREQ    BODE    [*]
PHASE    FREQ    BODE    [*]
IMAG    REAL    NYQUIST [ ]
GAIN    PHASE    NICHOLS [ ]
SCALE    LIMITS  CO-ORD
FREQ    [    ] [    ] HZ
GAIN    [    ] [    ]
PHASE    [    ] [    ] DEG
CHANNEL  PLOT A[*] B[ ] B/A[ ]
PHASE    +180[ ] 0-360[*]
                READY

```

FIGURE A5.5



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10223: Power Supply 1 Unit (E92106, D82076/01, PL82076/01)

NOTE: This supply superseded the original supply assembly 81221, introduced to the Issue 3 manual on Technical Bulletin No.137, dated January 1982. The above diagram and parts list numbers do not appear in the Issue 3 manual, but are part of this bulletin, to be inserted into the relevant sections of the manual - see NEW PAGES.

To remove spikes from the earthing +5V supply the following changes have been made to the new supply:

Capacitor C50, Stock No. CS32949, 0.01 μ F, -20% +80%, 50V connected between pins 2 and 4 of PL5, on Power Supply Board 2.

The junction of resistors R52 and R56 should connect to 0V.

Circuit Diagram E91206 raised to Issue 5
Assembly Diagram D82076/01 raised to Issue 3
Parts List PL82076/01 raised to Issue 3

10195: Correlator A/D Board (E82040, D82041, PL82041)

To prevent IC13D and IC11G mislocking, Opto Isolator IC11G has been changed from Hewlett Packard GN137 to Hewlett Packard HCPL2601, having improved noise immunity.

Circuit Diagram E82040 raised to Issue 9
Assembly Diagram D82041 raised to Issue 11
Parts List PL82041 raised to Issue 17

10240: Keyboard (E82085, PL82086)

To reduce the sensitivity of the power-on reset circuit to mains transients, resistor R15 has been changed from 10 k Ω to 8.45 k Ω .

Resistor R15 now:
Stk No: DS35817, 8.45 k Ω , 1%, 0.4W, MR25.

Circuit Diagram E82085 raised to Issue 9.
Parts List PL82086 raised to Issue 14.



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Modification(s)

C/N No(s)

9829: Display Monitor Module (D92370,D86872/01,PL86872/01)

As previously covered in Technical Bulletin No. 137, from contract No. 403145, the type 18 module is replaced by type 29A. The above diagram numbers do not appear in the Issue 3 manual, but are part of this bulletin, to be inserted into the relevant sections - see NEW PAGES below.

NEW PAGES

Power Supply Unit

Fig No.

E92106	Circuit Diagram	8.24A
E81221/01	Assembly Diagram	8.25A
D82071/01	Board No.1	8.26A
D82076/01	Board No.2	8.27A
D82081/01	Motherboard	8.28A

Page No.

PL81221/01	Power Supply Type 1	9.83
PL82081/01	Power Supply 1 Motherboard	9.87
PL82071/01	Power Supply Board No.1	9.89
PL82076/01	Power Supply Board No.2	9.91

Display Monitor Module

Fig No.

D82370	Circuit Diagram	8.18A
D86872/01	Assembly Diagram	8.19A

Page No.

PL86872/01	Monitor Module	9.80
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PREFACE

DAMAGE IN TRANSIT

Unpack the equipment and examine it thoroughly to ascertain whether any damage has occurred in transit. Report immediately any such damage to the agent or manufacturer. Retain the four rubberized packing surrounds, should a return to manufacturer be necessary.

GUARANTEE

All goods manufactured by the Company are guaranteed to the extent hereafter mentioned against defects arising from faulty material or workmanship subject to the goods not having suffered maltreatment or interference. The Company's liability under this guarantee is limited to replacing any part or parts found defective within a period as laid down in Company instructions after the date of delivery or installation.

If goods not of the Company's manufacture are ordered, the guarantee of that company is to be accepted.

LOCAL AGENTS ADDRESS

The address of your local agent is:

DESCRIPTIVE MATTER AND ILLUSTRATIONS

Descriptive matter, illustrations, dimensions and weights issued by the Company are typical and shall not be held as binding. The Company reserves the right to alter patterns and designs without notice.

SAFETY MEASURES

1. This instruction manual contains certain
— CAUTION — and — WARNING —
notices which *MUST* be followed by the user
to ensure *SAFE* operation and to retain the
equipment in a *SAFE* condition.
2. All users of the equipment described in this
manual *MUST* have received adequate training
in its use and application in order to ensure
SAFE AND PROPER USE.
3. Any adjustment, maintenance and repair of the
opened apparatus under voltage shall be
carried out only by a skilled person who is
AWARE OF THE HAZARD INVOLVED.
4. MEDICAL EQUIPMENT to be returned to SE Labs
(EMI) Ltd., *must* indicate that it has been
DE-CONTAMINATED.

FREQUENCY RESPONSE ANALYSER SE 2450

Manuals in this Series:

Operating & Servicing Instructions (MS 50093)

*Communications & General Purpose Interface Bus Option SE 2451
(MS 50105)*

External Synchronisation Option SE 2452 (MS 50108)

X-Y Plotter Option SE 2453 (MS 50106)

Graphic Display Option SE 2454 (MS 50107)

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SECTION 2	GENERAL INFORMATION
SECTION 3	INSTALLATION
SECTION 4	OPERATION
SECTION 5	SYSTEM DESCRIPTION
SECTION 6	CIRCUIT DESCRIPTIONS
SECTION 7	MAINTENANCE
SECTION 8	CIRCUIT & COMPONENTS LAYOUT DIAGRAMS
SECTION 9	PARTS LISTS

SECTION 1

SPECIFICATIONS

1. GENERATOR SECTION

Frequency:	Range:	0.0001Hz to 9999Hz.	
	Resolution:	May be set to any frequency within the range of 0.0001Hz to 9.999kHz to 4 digits.	
	Accuracy:	0.01% of reading.	
	Stability:	0.001% over 1 year.	
Amplitude Range:	1mV to 9.99V r.m.s. or peak.		
	Range	Resolution	
Resolution:	0.3125 V - 9.99V	10mV	
	0.03125V - 0.3124V	1mV	
	0.001 V - 0.03124V	0.1mV	
Accuracy of Setting:	0.3125 V - 9.99V	± 25mV	
	0.03125V - 0.3124V	± 4mV	
	0.001 V - 0.03124V	± 0.4mV	
Stability:	0.1% of reading.		
Waveshapes:	(a) sinewave (b) squarewave peak calibrated (c) triangular wave peak calibrated		
Waveform:	1024 steps/cycle.		
Output Impedance:	0.5Ω		
Output Current:	>5V 100mA <5V 200mA Short circuit protection.		
Background Noise:	>60dB below output level of 1V r.m.s.		
Harmonic Distortion:	2nd Harmonic	50dB)	below fundamental throughout frequency range
	3rd Harmonic	40dB)	
	4th Harmonic	50dB)	
	5th Harmonic	50dB)	

Output Bias:

Amplitude: -9.98V to 9.99V
Resolution: 10mV
Stability: 0.1%
Polarity: plus or minus with respect to generator
Lo terminal.

Frequency Sweep:

Range: Can be set to any frequency within the range
of 0.0001Hz to 9.999kHz to 4 digits.
Increments: Linear or logarithmic.
Sweep Distortion: Up or down.

Generator output is isolated from ground.

Maximum common-to-ground voltage: 500V

Generator settling time: 0.5s worst case.

Generator STOP/START: Modes : stop at 0°
stop at 90°
stop at 180°
stop at 270°

Measurement starts at specified STOP angles.

2. CORRELATOR SECTION

Each correlator has separate Hi, Lo and earth terminals. The Hi, Lo inputs are fully isolated from ground and the rest of the instrument.

Input Impedance: $1M\Omega \pm 0.1\%$ in shunt with approx 150pF.

Common Mode Rejection: 140dB at d.c.
60 dB at 50Hz for 1K unbalance.

Input Isolation between
Channels: 100dB

Measurement Capability:

Frequency Range: 0.0001Hz to 9999Hz

Harmonic Range: Up to 15
Frequency of harmonic to be less than
9999Hz.

The maximum harmonic number is given by:

Maximum Harmonic Number: Largest integer less than $\frac{9.9999\text{kHz}}{G}$

where G = generator frequency in kHz

Phase Accuracy: R > 10% for ranges 0.05V, 5V, 50V, 500V

0.0001Hz to 100Hz, 0.05°

100Hz to 1000Hz, 0.05° ± 0.01° /100Hz

1000Hz to 9999Hz, 0.14° ± 0.05° /1000Hz

R > 20% for range 0.05V

0.0001Hz to 100Hz, 0.1°

100Hz to 1000Hz, 0.1° ± 0.01° /100Hz

1000Hz to 9999Hz, 0.19° ± 0.05° /1000Hz

Amplitude, Real,

Imaginary, Accuracy:

0.001Hz to 5000Hz:

(± 0.15% of correlator range times 2) ± 0.1dB.

5000Hz to 9999Hz:

(± 0.3% of correlator range times 2) ± 0.2dB.

B/A Channel:

Matched to give accuracies comparable to single channels.

It is not advisable to use the instrument below 0.005V polar co-ordinates as the inaccuracies of deriving phase from cartesian co-ordinates becomes significant.

DC Offset Rejection

Manual or Automatic:

Integration Time: Minimum 100ms + time to complete number of cycles.

Integration Cycles: 1 to 9999.

Pre-Measurement Delay: 0.1s to 9999s

Range Detection:

Underrange:

the word 'underrange' flashes when an underrange is detected.

50mV range below 0.25%

0.5V, 5V, 50V, 500V range below 5%

Overrange:

the word 'overrange' flashes when an overrange is detected.

This is at 525V peak or r.m.s. as selected.

Input Amplifier:

Overrange Capability: 200% of full scale on all ranges.

Measurement Dynamic
Range (with auto-range,
without overranging: 500V to 300V r.m.s. or peak.

3. ENVIRONMENTAL

Temperature: 0° C to 40° C operating
-10° C to 70° C storage

Humidity: 10% to 90% non-condensing

4. POWER REQUIREMENTS

115V, +10%, -15%, 60Hz approx 2A
240V, +10%, -15%, 50Hz approx 1A

SECTION 2

GENERAL INFORMATION

Sub-Section	LIST OF CONTENTS	Page No.
1	Introduction	2.1
2	Summary of Facilities	2.3
3	Correlation Technique	2.5
4	Optional Facilities	2.6
5	Accessories	2.6

1. INTRODUCTION

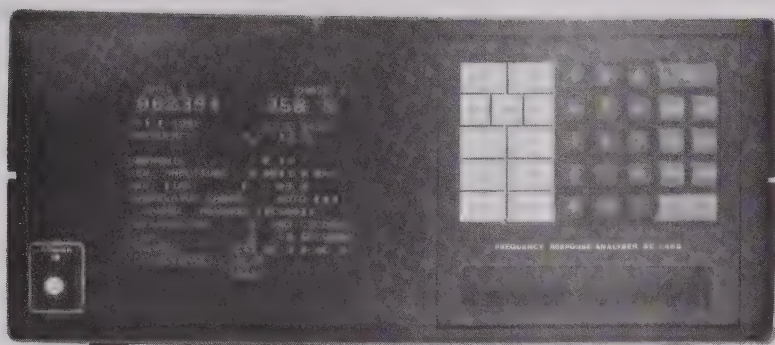
- 1.1 The SE 2450 Frequency Response Analyser (fig 2.1) is designed to measure the frequency response of dynamic systems. Electrical systems can usually be tested directly. Mechanical and hydraulic systems can be tested using transducers at the analyser and system outputs.
- 1.2 Control of the SE 2450 is simplified by the provision of a keyboard and a CRT display. The keyboard is used to enter the parameters of the excitation signal and the types of measurements required onto data pages displayed on the CRT. The results of the analyses are also displayed on the CRT. A remote programming facility is available.
- 1.3 There are 4 versions of the SE 2450 available:
- (a) SE 2450/00 - 230 V supply (EMI Front Panel)
 - (b) SE 2450/01 - 115 V supply (Customized Front Panel)
 - (c) SE 2450/04 - 230 V supply (Customized Front Panel)
 - (d) SE 2450/05 - 115 V supply (EMI Front Panel)

Interface boards are discussed in sub-section 4.

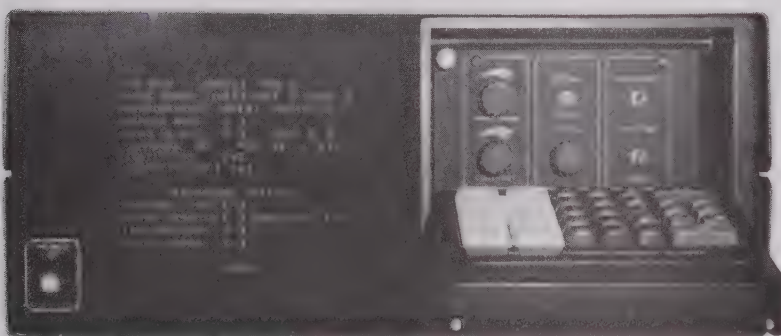
- 1.4 An internally generated sine, square or triangular waveform is used to excite the system under test the output of which is measured by a correlator to determine amplitude and phase relationships. Results can be displayed as:
- (a) quadrature and in-phase component in cartesian co-ordinates,
 - (b) modulus and phase angle in polar form or,
 - (c) log modulus and phase angle in log polar form.

There are 2 correlator channels in the instrument. It is therefore possible to obtain either absolute correlator results or the following results in the formats above:

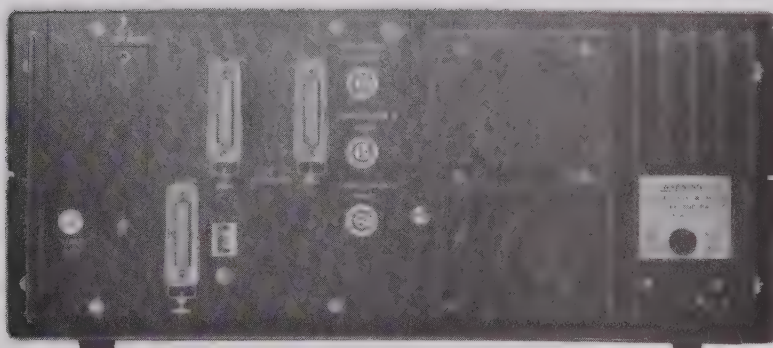
- (a) ratio of 2 correlator results or,
- (b) ratio of correlator input to generator output.



FRONT VIEW (KEYBOARD UP)



FRONT VIEW (KEYBOARD DOWN)



REAR VIEW

FIG. 2.1 SE2450 FREQUENCY RESPONSE ANALYSER

Statistical information is also provided as % standard deviation in all measurement modes except cartesian co-ordinates.

- 1.5 The SE 2450 has the further capability of making single measurements at a specified frequency or a sweep measurement over a frequency range selected by the user. Up to 120 results can be stored in the instrument for examination when required.
- 1.6 Fig 2.2 shows the types of computations leading to the various results obtainable. The system illustrated has a 2-channel correlator and is used in the single frequency measurement configuration.
- 1.7 Digital techniques are used throughout the instrument, ensuring high overall stability, resolution and accuracy. The correlation technique has the property of integrating out any noise that may be present in the system under test. Thus accurate results are obtained under severe noise level conditions. The statistical result gives an indication of the noise level present in the results obtained.

2. SUMMARY OF FACILITIES

- 2.1 Generator parameters which can be selected in single measurement mode are:

- (a) frequency,
- (b) amplitude expressed as either an r.m.s. or a peak voltage,
- (c) d.c. bias applied to the generator output,
- (d) sine, triangular or square waveshape.

In sweep measurement mode the above parameters can be selected as well as:

- (a) start and final frequencies,
- (b) number of frequency intervals,
- (c) linear or logarithmic sweep interval mode.

The generator phase stop facility allows the generator to be stopped at 0° , 90° , 180° or 270° in the cycle so that measurement can begin at this point.

- 2.2 The signal returned by the system under test is compared with the generator output. Two correlator channels are provided for which the following facilities can be selected:

- (a) type of measurement - real/imaginary, gain/phase, log gain/phase,
- (b) the harmonic of the generator frequency at which analysis is required,
- (c) manual or automatic correlator range selection. With automatic ranging, measurement begins at the most sensitive range and the instrument ranges up as necessary. Manual ranging saves time especially at low frequencies by allowing measurement to start at the appropriate range.

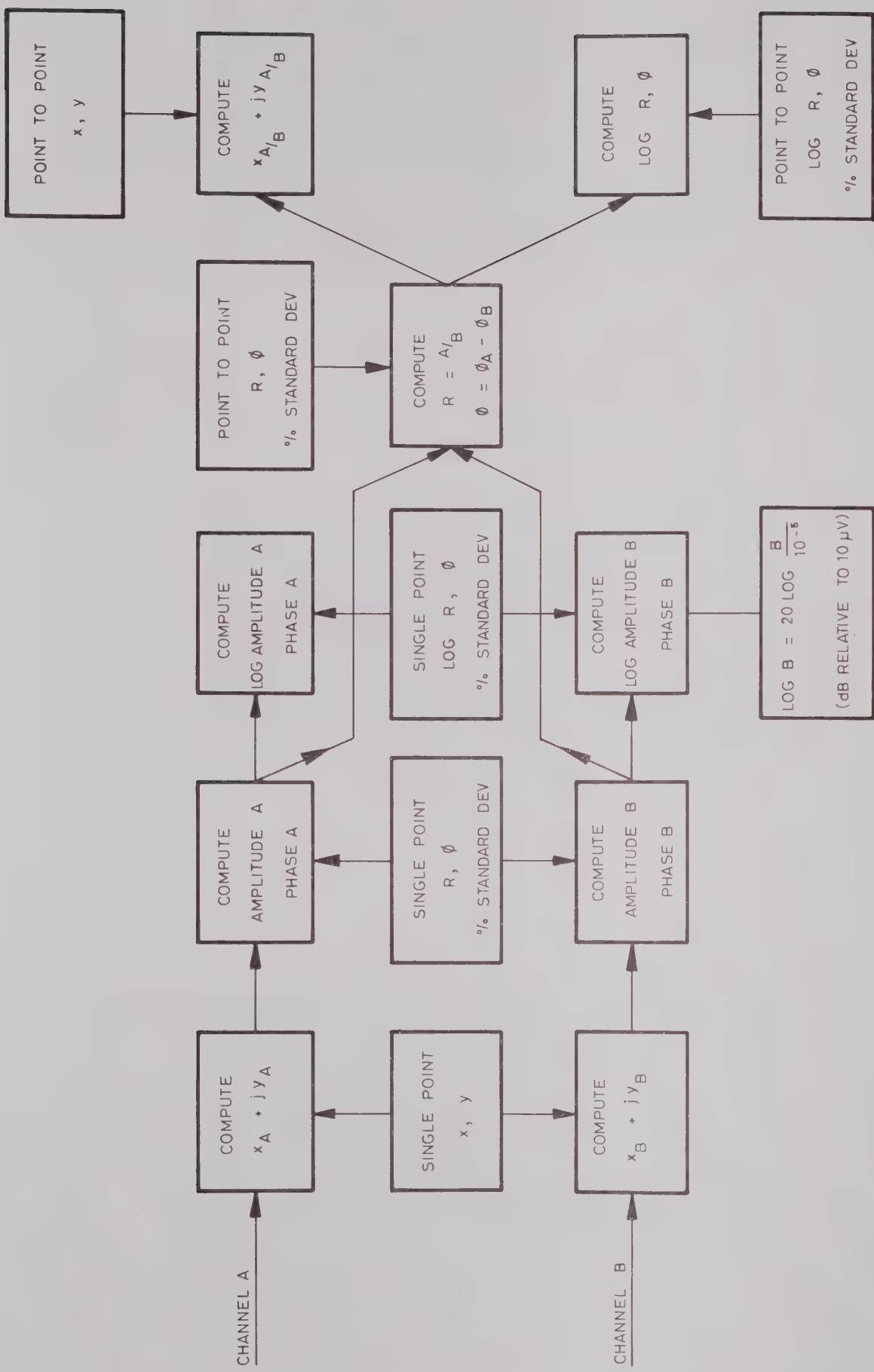


FIG. 2.2 TYPES OF COMPUTATION

- (d) r.m.s. or peak voltage measurement. The results obtained correspond to the generator setting, e.g. if the generator output is specified in r.m.s., the results is in r.m.s.
- (e) integration cycles - the number of generator cycles over which measurement is to be performed. This enables the operator to compromise between accuracy (noise rejection) and measurement time.
- (f) the correlator channel result required - A, B or B÷A.
- (g) the delay imposed between the generator starting and measurement beginning, to allow settling time in the system under test.
- (h) the type of result required - absolute correlator result or ratio of correlator result to generator output.
- (j) repeated measurement option - measurement is repeated and results are updated.
- (k) manually specified or automatically determined d.c. bias rejection in returned signal. As with manual range selection, manual bias selection minimises measurement time especially at low frequencies.
- (m) statistical analysis (% standard deviation) - a useful indicator of the credence of results obtained when analysing an electrically noisy system.
- (n) pause facility - allows measurement to be interrupted in order to change certain (unprotected) parameters.

2.3 Types of interface available with the analyser include an external sync unit, RS 232 interface, X-Y plotter, remote display and IEEE-488. Outputs to certain peripherals can be selected via the keyboard.

2.4 The instrument can be operated on mains supply voltage of 115 V, +10%, -15% or 230 V, +10%, -15%, 45-65 Hz.

3. CORRELATION TECHNIQUE

3.1 The correlation technique is used for measuring the real and imaginary parts of the signal. The information is then used for deriving the amplitude, phase, etc., as required by the operator. It can be shown that:

$$X_A = \frac{1}{nT} \int_0^{nT} V_{\max} \sin(\omega t + \phi) \sin \omega t \, dt$$

$$Y_A = \frac{1}{nT} \int_0^{nT} V_{\max} \sin(\omega t + \phi) \cos \omega t \, dt$$

where X_A =	real part in volts	ϕ =	phase shift of correlator input signal relative to generator output
nT =	integration time		
$V_{\max}$ =	peak of correlator input signal	Y_A =	imaginary part in volts

- 3.2 In order to get a reasonably high sample rate (to improve accuracy) in a given time it is necessary to select a fast rate of sampling (48 kHz). It is therefore necessary to compute $V_{\max} \sin(\omega t + \phi) \sin \omega t$ and add it to the previous result and also to compute $V_{\max} \sin(\omega t + \phi) \cos \omega t$ and add it to the previous result in 0.02ms.
- 3.3 This is too fast for the software to handle, therefore these computations are performed by hardware. The results of 256 samples (a block) are added together and stored in a register, see fig 2.3. The software then stores the result of this block and adds it to the previous block. When the required number of blocks has accumulated, the software divides this overall result by a constant and real and imaginary parts are obtained.
- 3.4 In most cases the number of integration cycles is not directly divisible by a block. It is therefore necessary to select part of a block to complete the correct number of integration cycles. This is computed by the software and loaded into a register which controls the number of samples to be performed in the incomplete block which is done first.

4. OPTIONAL FACILITIES

4.1 Communications and General Purpose Interface Bus Option SE 2451

4.1.1 This board contains two separate and independent interfaces as follows:

- (a) **Serial Interface.** This enables a printer such as a Teletype or other serial input device to be interfaced to the SE 2450 via socket SKT38 on the rear panel. Provision is made for asynchronous operation up to 9600 Baud.
- (b) **IEEE 488 (parallel) Interface.** This enables the SE 2450 to communicate with any other instrument equipped with a suitable interface via the IEEE 488 G.P.I.B. Access to the bus is via the rear panel socket SKT40.

4.1.2 With this option, the SE 2450 can operate as a talker or listener; it cannot act as a controller. When the SE 2450 is being controlled remotely via the bus, the serial interface is inhibited. Refer to the relevant option manual.

4.2 External Synchronisation Option SE 2452

4.2.1 This option enables the SE 2450 to perform its measurements in synchronisation with some external event. For example, it may be required to perform a measurement on a rotating machine at a particular point in its rotation or at a known rotation speed.

4.2.2 The external sync. option accepts an electrical trigger pulse generated by the machine and uses it to synchronise the measurement circuits of the SE 2450. It also measures the time interval between successive trigger pulses and displays this as a frequency. Refer to the relevant Option Manual.

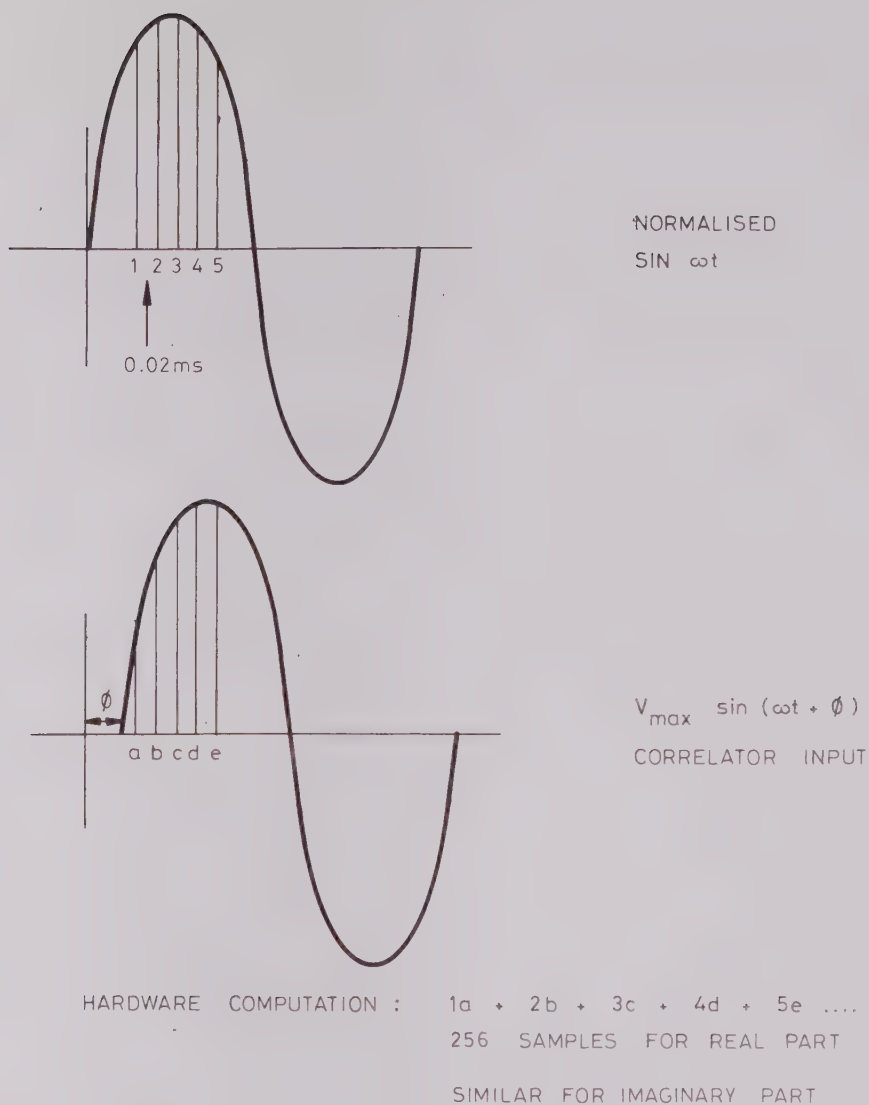


FIG. 2.3 HARDWARE SAMPLING

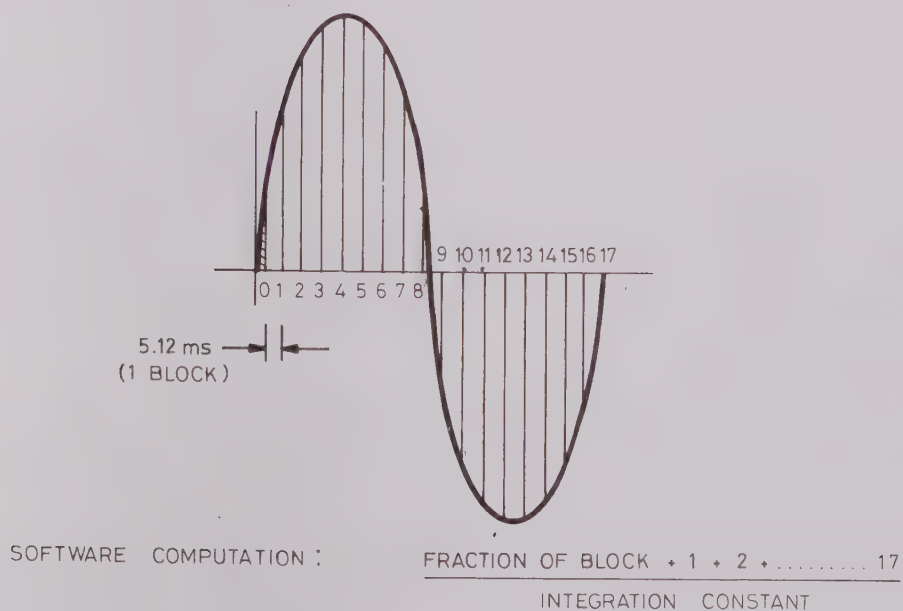


FIG. 2.4 SOFTWARE COMPUTATION

4.3 X-Y Plotter Option SE 2453

- 4.3.1 This option allows the SE 2450 to plot the measured results in graphical form on an external X-Y plotter, connected to the SE 2450 via the IEEE 488 Interface socket SKT40 on the rear panel, provided Option SE 2451 (above) has also been installed.
- 4.3.2 The additional software provided with this option enables the SE 2450 to drive three types of X-Y plotter; Hewlett Packard models 7225A, 9872A and 9872B. If H.P.9872A is to be used, then the SE Labs Listen Address Box C91412 is also required.

4.4 Alphanumerics Control Board Option

- 4.4.1 This board contains most of the facilities originally contained on two display control boards in the basic SE 2450/00 and SE 2450/01 versions and is a replacement for the pair. Fitment of this option allows the graphic option (below) to be subsequently fitted. Operation of the SE 2450 is unaffected by fitting the alphanumeric control board; only the appearance of the display is affected. The full 128 ASCII character set is contained on the board, including upper and lower case characters and control characters.
- 4.4.2 A cursor can be displayed together with any character in any position, the display alternating between character and cursor once per second. A group of consecutive characters can be made to flash or can be displayed bright or dim.

4.5 Graphics Control Board Option SE 2454

- 4.5.1 The SE 2450 can be supplied with an option enabling it to plot the measured results in graphical form on the screen. The basic SE 2450 contains 2 display control boards which must be replaced by the alphanumeric control board (described above) and a graphics control board. This option also requires additional graphics software to be installed.
- 4.5.2 When this option has been installed, an extra data entry page is provided. This is used to specify the type of graph plot which can be presented by an on-screen graphics display page. The SE 2450 is used in the sweep frequency mode. After a normal measurement sequence, up to 120 sets of results are stored. These are then converted into the units required for plotting and presented in graphical form by the software. Refer to the relevant options manual.

4.6 Video Output

The CRT display is also output for a remote monitor.

4.7 Options Socket

An additional 25-way socket is provided on the back panel and is wired to a spare p.c.board slot on the motherboard. This socket is provided so that other interfaces can be added.

5. ACCESSORIES

5.1 Rack Mounting Kit E82755

This is a tray assembly with slides used to mount the SE 2450 in a 19-inch wide by 24-inch deep rack.

SECTION 3

INSTALLATION

Sub-Section	LIST OF CONTENTS	Page No.
1	Introduction	3.1
2	Unpacking	3.1
3	Accessory Kit	3.1
4	Mounting	3.1
5	Connecting the Analyser	3.2
	Mains Voltage Selection	3.2
	Mains (Power) Connection	3.2
	Summary of Interface Connectors	3.3

1. INTRODUCTION

This section contains all the information necessary to install and connect the Frequency Response Analyser SE 2450.

2. UNPACKING

The instrument is supplied sealed in a polythene bag and is surrounded by rubber packing blocks. These should be retained for use when further transportation is necessary.

3. ACCESSORY KIT

The following items are supplied as standard with each Frequency Response Analyser SE 2450:

- (a) SE 2450 Instruction manual - 1 off
- (b) Connectors as follows:
 - (i) 3-pole Sealelectro-Fischer plug - 2 off
 - (ii) 4-pole Sealelectro-Fischer plug - 1 off
 - (iii) Belling Lee 4 mm plug (green) - 3 off
 - (iv) Belling Lee 4 mm plug (red) - 3 off
 - (v) Belling Lee 4 mm plug (black) - 3 off
- (c) Dust cover
- (d) Spare fuses as follows:
 - (i) FS1 : 2A (230V) or 4A (115V) - 1 off
 - (ii) FS11, FS12 : 2.5A (1-off), 4A - 1 off
 - (iii) FS13 : 15A

4. MOUNTING

The SE 2450 can be bench or rack mounted. Rack sliding supports are fitted to the sides of the instrument and an alternative extended front panel enables it to be held in place on the rack. This system is available in kit form as an optional extra (part number E82755).

5. CONNECTING THE ANALYSER

5.1 Mains Voltage Selection

The SE 2450 can be operated on mains voltages of 115 V or 230 V r.m.s., 45-65 Hz. It is important, therefore, to check the position of the mains voltage selection switch (SW2) and the rating of the mains fuse (FS1) on the back panel prior to connection to the mains. In order to check or change the setting of SW2, proceed as follows:

----- WARNING -----

VERY HIGH VOLTAGES are present inside the instrument cabinet while power is switched on and for a period after switching off. EHT for the display is generated in the area just in front of the PSU compartment.

DO NOT change the setting of the mains voltage selector switch with power switched on.

- (a) Loosen the 2 screw fasteners : 1 behind the keyboard and 1 at the top centre of the back panel.
- (b) Lift off the top cover.
- (c) SW2 is located on the front partition of the left rear (PSU) compartment inside the instrument. The switch is held in its set position by a locking plate which must be removed before the switch position can be changed. The mains voltage selected is indicated on the locking plate when in situ.

5.2 Mains (Power) Connection

The mains lead should be wired to a suitable mains plug as follows:

WIRE COLOUR	FUNCTION
Brown	Live
Blue	Neutral
Yellow/Green	Earth

5.3 Summary of Interface Connectors

5.3.1 Input Panel (right side)

(a)	Generator output Hi (red)	}	Belling Lee 4 mm sockets
(b)	Generator output Lo (black)		
(c)	Generator output E (green)		
(d)	Correlator A input Hi (red)		
(e)	Correlator A input Lo (black)		
(f)	Correlator A input E (green)		
(g)	Correlator B input Hi (red)		
(h)	Correlator B input Lo (black)		
(j)	Correlator B input E (green)		

5.3.2 Back Panel (fig 3.1)

(a)	Bus Extender - provision for optional addition of extender unit	
(b)	Video Output - BNC coaxial socket	
(c)	External Sync - Cannon D-type 25-way socket (for connection of external sync unit).	
(d)	RS232 Interface	} Cannon D-type 25-way sockets
(e)	SKT41 (options)	
(f)	IEEE-488 Interface - Amp Champ 24-way socket	
(g)	Generator Output - Sealelectro-Fischer 4-way socket	
(h)	Correlator A Input	} Sealelectro-Fischer 3-way sockets
(j)	Correlator B Input	
(k)	E (earth) - hex nuts	

Fig 3.1 shows the locations and pin numbering of the back panel connectors. Table 3.1 gives the pin allocations of SKT38,SKT39 and SKT40.

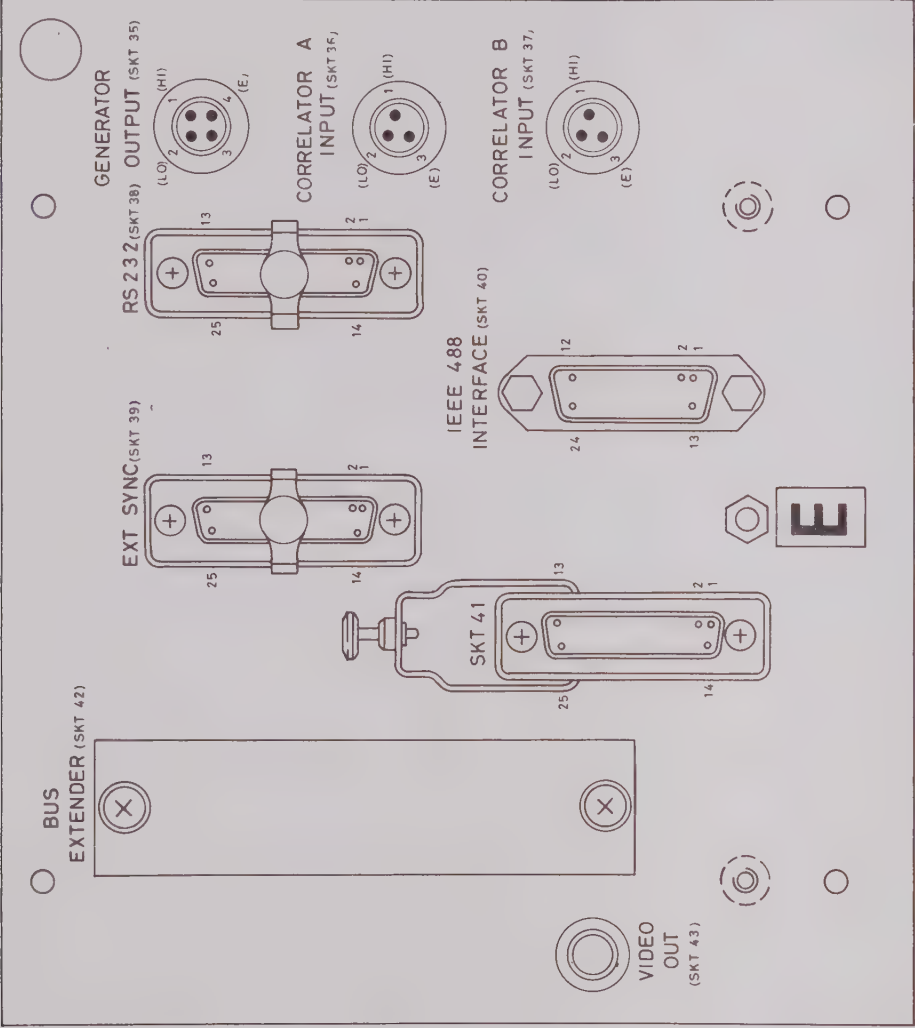


FIG. 3.1 BACK PANEL -INTERFACE CONNECTORS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	SCREEN	1	0 V (E)	1	DIO 1
2	TXD	2	+5 V (E)	2	DIO 2
3	RECEIVED DATA	3	-30 V (F)	3	DIO 3
4	RTS	4	0 V (F)A	4	DIO 4
5	CTS	5	+30 V (F)	5	EOI
6	DSR	6	SYNC CLK +	6	DAV
7	0 V (SIGNAL GND)	7	0 V (E)	7	NRFD
8	ATP2	8	+5 V (E)	8	NDAC
9	-	9	-30 V (F)	9	IFC
10	-	10	0 V (F)A	10	SRQ
11	-	11	+30 V (F)	11	ATN
12	-	12	SYNC CLK -	12	SHIELD
13	-	13	-	13	DIO 5
14	-	14	-	14	DIO 6
15	-	15	-	15	DIO 7
16	TTY READER CONTROL	16	-	16	DIO 8
17	-	17	-	17	REN
18	-	18	-	18	DAV GND
19	-	19	-	19	NRFD GND
20	DTR	20	-	20	NDAC GND
21	TTY RD.CONT.RETURN	21	-	21	IFC GND
22	-	22	-	22	SRQ GND
23	-	23	-	23	ATN GND
24	TTY RX RETURN	24	-	24	Data Bus GND
25	TTY TX RETURN	25	-		
RS 232 (SKT 38)		EXTERNAL SYNC (SKT 39)		IEEE-488 (SKT 40)	
See SE2451 Manual for connections					

TABLE 3.1 INTERFACE CONNECTOR PIN ALLOCATIONS

MANDATORY SETTINGS

SWITCH		POSITION	SWITCH		POSITION
ADD SEL 1: S1		OFF	INT REQ 1: S21		OFF
S2		OFF	S22		OFF
S3		OFF	S23		OFF
S4		ON	S24		OFF
S5		ON	S25		ON
S6		ON	S26		OFF
S7		OFF	S27		OFF
S8		OFF	S28		OFF

OPTIONAL SETTINGS

BAUD RATE	LINK	S11	S12	S13	S14	S15	S16	S17	S18
110	LK 4B	OFF	ON	ON	OFF	ON	OFF	ON	OFF
150	LK 4B	ON	ON	ON	ON	ON	ON	OFF	OFF
300	LK 4B	ON	ON	ON	ON	ON	OFF	OFF	OFF
600	LK 4B	ON	ON	ON	ON	OFF	OFF	OFF	OFF
1200	LK 4B	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
2400	LK 4B	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
4800	LK 4B	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
9600	LK 4A	ANY POSITION							

ADDITIONAL LINKS

RS 232C : Link LK 2B and LK 3B
Teletype : Link LK 2A and LK 3A
OV to screen : Link LK 1
OV not to screen: Link LK1 to PK (PARK)

TABLE 3.2 COMMUNICATIONS INTERFACE BOARD (POSITION NO 8)
- TELETYPE & RS 232C (Serial) INTERFACE (Switch & Link Positions)

SECTION 4

OPERATION

Sub-Section	LIST OF CONTENTS	Page No.
1	Introduction	4.1
2	CRT Data Display Pages	4.1
3	Summary of Control Keys	4.3
4	Control Panel	4.4
5	Operating Instructions	4.4
	Setting Up	4.4
	General Operating Notes	4.5
	Single Frequency Measurement	4.6
	Sweep Frequency Measurement	4.11
	Measurement Sequence	4.14
6	Operational Maintenance	4.17
	Input-Output Cableform	4.17
	PSU Fuses and Indicators	4.17
	Preset Display Controls	4.17

1. INTRODUCTION

Control of the SE 2450 is effected via the numerical/function keypad which is used to make the appropriate entries on the CRT data display. There are 3 data entry pages which are used to specify the excitation signal parameters and the type of analysis required. A number of results pages are available for displaying sweep frequency results.

2. CRT DATA DISPLAY PAGES

- 2.1 Data entry page 1(form 1) shown in fig 4.1 deals with the parameters and results relating to a single frequency analysis. The parameters for a sweep frequency analysis are entered on data entry page 2 (form 2) shown in fig 4.6. Up to 120 results of a sweep frequency analysis are displayed on 10 results pages, the format of which is given in fig 4.8. Options available for both single frequency and sweep frequency analysis including peripheral access can be specified on the options page shown in fig 4.2.
- 2.2 The various data entry and results pages are selected for display by the keys as explained below. A flashing cursor indicates the next position where data can be entered. The cursor can be positioned by the keys below.
- 2.3 Table 4.1 shows the various parameters, their ranges and the default conditions which are selected automatically upon switch-on. The table also shows which parameters are protected and which are unprotected. Unprotected parameters can be changed after interrupting measurement with the PAUSE key. The unprotected parameters appear brighter on the screen at this time.
- 2.4 The status of the instrument, i.e. READY, MEASURE, PAUSE, OVERRANGE or UNDERANGE is shown at the bottom of the screen.

DATA ENTRY FIELD	MEASUREMENT		RANGE		DEFAULT VALUE
	SINGLE	SWEEP	MIN	MAX	
FREQUENCY (single)	P	-	0.0001 Hz	9999 Hz	1 Hz
START FREQUENCY	-	P	0.0001 Hz	9999 Hz	1 Hz
FINAL FREQUENCY	-	P	0.0001 Hz	9999 Hz	100 Hz
HARMONIC	P	P	1	15	1
GEN.AMPLITUDE	P	P	0.001 V	9.99 V	0.001 V
GEN.BIAS	U	U	-9.99 V	+9.98 V	0V
CORR.RANGE (AUTO/manual)	U	U	-	-	AUTO
CHAN.A,CHAN B.(range)	U	U	0.05 V	500 V	500 V
INTEGRATION (CYCLES)	U	U	1	9999	10
DELAY	U	U	0.1 s	9999 s	0.5 s
INTERVALS	-	P	1	120	20
INTERVAL MODE (LINEAR/LOG)	-	U	-	-	LINEAR
CHANNEL (A,B,B/A)	P	P	-	-	A
CO-ORDINATES(CARTESIAN/POLAR/ LOG-POLAR)	U	U	-	-	POLAR
VOLTAGE (RMS/PK)	P	P	-	-	RMS
WAVE SHAPE (SIN/TRI/SQR)	U	U	-	-	SIN
MEASUREMENT (ABS/RATIO)	P	P	-	-	ABS
REPEAT MODE	U	U	-	-	Not Set
BIAS REJ	U	U	-	-	Not Set
AUTO/manual (BIAS REJ)	U	U	-	-	Manual
CHAN A,CHAN B. (BIAS REJ)	U	U	-500 V	+500 V	0 V
STATISTICS	U	U	-	-	Not Set
REPETITIONS	U	U	10	100	20
EXTERNAL SYNC	P	-	-	-	Not Set
PRINT RESULTS	U	U	-	-	Not Set
DUMP PAGE	P	P	0	5	0
X-Y PLOTTER	P	P	-	-	Not Set
MODE (single/sweep)	P	P	-	-	single

P = Protected

U = Unprotected

- = Not Applicable

TABLE 4.1 PARAMETER RANGES

2.5 If the data entered is incorrect in any way, when measurement starts, the field with the incorrect entry flashes and measurement ceases. This applies to:

- (a) a required data field left blank,
- (b) incorrect data format (spaces left in the middle of a data field, etc),
- (c) any parameter selected which is outside the range or resolution of the instrument.

3. SUMMARY OF CONTROL KEYS (FIG 4.5)

- | | |
|---|--|
| 3.1 DATA DISPLAY
and
ROLL keys | DATA DISPLAY key selects the format in which data is to be displayed: form 1 for single frequency measurements or results page(s) for sweep mode.

In sweep mode the ROLL key selects results pages consecutively up to page 10. |
| 3.2 DATA ENTRY,
FORM, Numeric
and ROLL keys | Pressing DATA ENTRY, FORM and '1' keys selects data entry page 1 for entering single frequency measurement parameters.

DATA ENTRY, FORM and '2' keys select data entry page 2 for entering sweep frequency parameters.

Pressing ROLL key causes options page to be displayed. Subsequently pressing ROLL causes display to revert to data entry page 1 or 2 as previously selected.(See also SE2453/SE2454 Manuals). |
| 3.3 R,Ø
a,b and
Log R,Ø keys | Select the co-ordinates in which data is to be displayed; polar, cartesian or log-polar respectively. |
| 3.4 Cursor control keys | |
| INT CYCLES
VOLTS OUTPUT
FREQ.
HARMONIC | } Position cursor under m.s.d. of corresponding field. |
| TAB+
TAB- | } Move cursor to m.s.d. of next or previous field. Positions of these keys are transposed on units marked SE 2460/03 & SE 2461/02. |
| →
← | } Move cursor to next or previous digit entry position. |
| 3.5 Numeric keys
0,1,2,3,4,5,6,8,9 | } Used as required to specify data entry form number and parameters. |
| 3.6 * (asterisk) key | Used in a single character field when a mode is being selected, e.g. AUTO (*). |

- 3.7 +, - keys Used to indicate polarity of specified voltages.
- 3.8 SPACE key Leaves the cursor position blank (erases) and moves cursor to next digit entry position.
- 3.9 START key Starts measurement.
- 3.10 SHIFT key Used with numeric keys to set generator to the point in the cycle at which measurement is to begin:
 - SHIFT,0 = 0°
 - SHIFT,1 = 90°
 - SHIFT,2 = 180°
 - SHIFT,3 = 270°
- 3.11 PAUSE key Interrupts measurement, allowing unprotected parameters to be changed.
- 3.12 STOP key Unconditionally stops measurement.

4. CONTROL PANEL

- 4.1 The control panel located behind the keyboard contains the 3 control groups explained below from left to right. The keyboard is pulled forward from the bottom for access to the control panel.
 - 4.1.1 *Display Picture Controls.* These comprise brightness and contrast potentiometers for the display.
 - 4.1.2 *Generator D.C. Offset.* This consists of a manual/auto switch which selects the source of the generator offset voltage: the potentiometer below the switch or the keyboard, respectively. When the potentiometer is used to set the offset voltage, the operator must monitor the generator output externally.
 - 4.1.3 *Additional Functions.* The upper switch is used to implement a diagnostic software routine. The lower switch, biased away from the LOCAL position, is momentarily switched to LOCAL in order to regain local control of the instrument after it has been controlled remotely.

5. OPERATING INSTRUCTIONS

5.1 Setting Up

- (a) Ensure that the instrument has been set correctly for the local (mains) power source (refer to Part 3, para 5.1) and that the correct value of mains fuse (FS1) has been inserted in the back panel (see fig 4.11).

- (b) Connect the generator output to the input of the equipment to be analysed via either the input panel (on the right-hand side of the instrument) or the back panel (refer to Part 3, para 5.3). Alternatively, to check the instrument operationally, connect the generator output directly to either correlator input on the input-output panel.
- (c) Connect the output(s) of the equipment to be analysed to the correlator input(s) as required via either the input panel or the back panel.
- (d) Switch power on at the lower left-hand corner of the front panel. The l.e.d. indicator lights when mains power is switched on. Allow 15 minutes to elapse before attempting to take a measurement.
- (e) The display (fig 4.1) should appear within 20s; if not, check the adjustment of the brightness and contrast controls behind the keyboard. Pull the keyboard forward from the bottom for access to the control panel.
- (f) If the display is not steady and synchronised, refer to para 6.3 below.

5.2 General Operating Notes

The user is advised to read the notes and the operational procedures below in their entirety before attempting to operate the instrument.

- (a) Upon switch-on the flashing cursor which indicates the digit position ready to receive data is at the m.s.d. of the FREQUENCY field.
- (b) The default values shown in table 4.1 are entered automatically upon switch-on. These values are simply overwritten or erased with the SPACE key when entering parameters.
- (c) The default values or parameters remaining from a previous measurement cycle continue to be effective if left unchanged.
- (d) Values left in manual parameter fields (CORRELATOR RANGE and BIAS REJECT) are ineffective if automatic range and bias are selected. This also applies to REPETITIONS if STATISTICS is not selected.
- (e) Data must be entered such that no spaces are left between characters in a field.
- (f) The generator output is set to the selected values when the START key is pressed.
- (g) The results of a measurement cycle remain displayed until the START key is pressed to initiate a new measurement cycle.
- (h) When switching between absolute and ratio measurement, the labelling of results may not appear correct until the START key is pressed.
- (j) An up or down sweep frequency analysis can be made by entering appropriate start and final frequencies.

5.3 Single Frequency Measurement (figs 4.1 & 4.2)

5.3.1 *Entering Generator Parameters*

- (a) Data Entry Form 1 is displayed upon switch-on.
- (b) To display this form, when another page is being displayed, press keys DATA ENTRY, FORM and 1.
- (c) Enter the generator FREQUENCY (0.0001 Hz - 9999 Hz).
- (d) Enter the GEN.AMPLITUDE (0.001 V - 9.99 V).
- (e) Enter the GEN.BIAS (between -9.99 V and +9.98 V).
(Alternatively, generator bias can be set on the control panel - see sub-section 4).
- (f) Press the ROLL key to display the Options Page below.

Reference Fig 4.2:

- (g) Specify with an asterisk (*) whether the generator amplitude is expressed as an RMS or a PEAK voltage. (This also determines how the results are expressed).
- (h) Select with an asterisk (*) SIN (sine), TRI (triangular) or SQR (square) waveshape.
- (j) If it is desired to begin the measurement at a particular point in the cycle, i.e. 0°, 90°, 180° or 270°, the generator is stopped to restart at this point by pressing the SHIFT key followed by the 0, 1, 2 or 3 key, respectively.
- (k) Press the ROLL key to display Data Entry Form 1 and proceed to para 5.3.2.

GENERATOR PARAMETERS (SINGLE FREQUENCY MEASUREMENT)

TO DISPLAY THIS FORM : PRESS KEYS DATA ENTRY FORM 1

A M P L V										P H A S E °																			
⊘	.	5	⊘	⊘	⊘	⊘				⊘	.	⊘	⊘	⊘															
S 1					[0 . 1]					%					S 2					[0 . 5]					%				
F R E Q U E N C Y										[					1]					H z									
H A R M O N I C										[					1]														
G E N .					A M P L I T U D E										[. 5 0 0]					V R M S									
G E N .					B I A S										[3 . 0 0]					V									
C O R R E L A T O R										R A N G E										A U T O					[*]				
C H A N N E L										A [5 0 0]					V					B [5 0 0]					V				
I N T E G R A T I O N										[					1 0]					C Y C L E S									
D E L A Y										[					. 5]					S E C O N D S									
C H A N N E L										A [*]					B []					B / A []									
C O - O R D I N A T E S										P O L A R																			
										R E A D Y																			

FIG. 4.1 DATA ENTRY FORM 1

TO DISPLAY THIS PAGE : PRESS ROLL

V O L T A G E										R M S [*]					P E A K []																								
W A V E S H A P E										S I N C [*]					T R I C []					S Q R C []																			
M E A S U R E M E N T										A B S C [*]					R A T I O C []																								
R E P E A T M O D E										[*]																													
B I A S R E J E C T										[]					A U T O					[*]																			
C H A N N E L										A [					0]					V					B [					0]					V				
S T A T I S T I C S										[*]																													
R E P E T I T I O N S										[1 0]																													
										P E R I P H E R A L O P T I O N S																													
E X T E R N A L S Y N C										[]																													
P R I N T R E S U L T S										[]					D U M P P A G E					[]																			
X Y P L O T T E R										[]																													
										R E A D Y																													

FIG. 4.2 OPTIONS PAGE

NOTE
GRID LINES SHOWN FOR CLARITY

5.3.2 *Entering Correlator Parameters (figs 4.3 & 4.4)*

- (a) Enter the number of the HARMONIC of the generator frequency at which analysis is required (1-15, but selected harmonic must be 9999 Hz or less).
- (b) Specify with an asterisk (*) CORRELATOR RANGE AUTO if required.
- (c) Enter the correlator range for each CHANNEL as required if automatic ranging is not being performed (0.05 V - 500 V).
- (d) Enter in INTEGRATION CYCLES the number of generator cycles over which measurement is to be made (1-9999).
- (e) Enter the DELAY to be imposed between the generator starting and measurement beginning (0.1s - 9999s).
- (f) Specify with an asterisk (*) the correlator CHANNEL(s) from which a result is required.
- (g) Refer to para 5.3.3 for the selection of CO-ORDINATES.
- (h) Press the ROLL key to display the Options Page below.

Reference fig 4.4:

- (j) Specify with an asterisk (*) whether the MEASUREMENT is to give an absolute (ABS) correlator result or a RATIO of correlator input to generator output.
- (k) Specify with an asterisk (*) if REPEAT MODE (automatic repetition of measurement) is required.
- (m) Specify with an asterisk (*) if BIAS REJECT(ion) at the correlator input(s) is required and if AUTO(matic) bias rejection is to apply.
- (n) Enter manually-selected d.c. levels to be rejected as required (between -500 V and +500 V).
- (p) Specify with an asterisk (*) if STATISTICS (% standard deviation) are required in addition to other results specified. (Not applicable when results are given in cartesian co-ordinates).
- (q) Enter the number of REPETITIONS of the specified measurement required for obtaining the statistical result (10-100).
- (r) Specify with asterisks (*) the PERIPHERAL OPTIONS required (if equipped).
- (s) Press the ROLL key to display Data Entry Form 1 when results are also displayed.
- (t) Press the START key to start measurement.
- (u) Refer to para 5.5.

CORRELATOR PARAMETERS

(SINGLE FREQUENCY MEASUREMENT)

TO DISPLAY THIS FORM : PRESS KEYS

DATA
ENTRY

FORM

1

AMPL V										PHASE °									
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5		
S1 [0.1] %										S2 [0.5] %									
FREQUENCY										1 Hz									
HARMONIC										1									
GEN. AMPLITUDE										.500 V RMS									
GEN. BIAS										3.00 V									
CORRELATOR RANGE										AUTO [*]									
CHANNEL AC 500 V										BC 500 V									
INTEGRATION										10 CYCLES									
DELAY										.5 SECONDS									
CHANNEL										AC [*] BC B/AC									
CO-ORDINATES										POLAR									
READY																			

FIG. 4.3 DATA ENTRY FORM 1

TO DISPLAY THIS PAGE : PRESS

ROLL

VOLTAGE										RMS [*]										PEAK																			
WAVE SHAPE										SIN [*]										TRI										SQRC									
MEASUREMENT										ABS [*]										RATIO																			
REPEAT MODE										[*]																													
BIAS REJECT										[]										AUTO [*]																			
CHANNEL AC										0 V										BC 0 V																			
STATISTICS										[*]																													
REPETITIONS										10																													
PERIPHERAL OPTIONS																																							
EXTERNAL SYNC										[]																													
PRINT RESULTS										[]										DUMP PAGE []																			
X-Y PLOTTER										[]																													
READY																																							

FIG. 4.4 OPTIONS PAGE

NOTE

GRID LINES SHOWN FOR CLARITY

[illegible][illegible][illegible]

	G	A	I	N											P	H	A	S	E	O
--	---	---	---	---	--	--	--	--	--	--	--	--	--	--	---	---	---	---	---	---

[illegible]

FIG.4.5 RESULT LABELLING - FORM 1
(SINGLE FREQUENCY MEASUREMENT)

5.3.3 Selection of CO-ORDINATES

Fig 4.5 above shows the labelling of results at the top of Form 1 for each type of co-ordinates and measurement.

- (a) To select cartesian co-ordinates,press the a,b key.
- (b) To select log-polar co-ordinates,press the Log R, ϕ key.
- (c) To select polar co-ordinates,press the R, ϕ key.

The selection of ABS or RATIO results is made as explained in para 5.3.2 (j).'

GENERATOR PARAMETERS (SWEEP FREQUENCY MEASUREMENTS)

TO DISPLAY THIS FORM : PRESS KEYS

DATA
ENTRY

FORM

2

S	T	A	R	T	F	R	E	Q	U	E	N	C	Y	[	1	0	0	.	5	]	H	Z				
F	I	N	A	L	F	R	E	Q	U	E	N	C	Y	[	9	9	9	9	]	H	Z					
H	A	R	M	O	N	I	C						[	1	]											
G	E	N	.	A	M	P	L	I	T	U	D	E		[	5	.	0	0	]	V	R	M	S			
G	E	N	.	B	I	A	S						[				0	]	V							
C	O	R	R	E	L	A	T	O	R	R	A	N	G	E					A	U	T	O	[	*	]	
C	H	A	N	N	E	L		A	[	5	0	0	]	V		B	[	5	0	0	]	V				
I	N	T	E	G	R	A	T	I	O	N				[		1	0	]	C	Y	C	L	E	S		
D	E	L	A	Y									[			.	2	]	S	E	C	O	N	D	S	
I	N	T	E	R	V	A	L	S					[		1	2	]									
I	N	T	E	R	V	A	L	M	O	D	E	L	I	N	E	A	R	[	*	]	L	O	G	[		]
C	H	A	N	N	E	L					A	[		]	B	[	*	]	B	/	A	[		]		
C	O	-	O	R	D	I	N	A	T	E	S		P	O	L	A	R									
												R	E	A	D	Y										

FIG. 4.6 DATA ENTRY FORM 2

5.4 Sweep Frequency Measurement

5.4.1 Entering Generator Parameters

- (a) To display this form,press keys DATA ENTRY,FORM and 2.
- (b) Enter the START FREQUENCY (0.0001 Hz - 9999 Hz).
- (c) Enter the FINAL FREQUENCY (0.0001 Hz - 9999 Hz).
- (d) Enter the GEN.AMPLITUDE (0.001 V - 9.99 V).
- (e) Enter the GEN.BIAS (between -9.99 V and +9.98 V). (Alternatively, generator bias can be set on the control panel - see sub-section 4).
- (f) Enter in the INTERVALS field the number of frequencies to be analysed during the sweep. (Intervals between frequencies must be 0.0001 Hz or greater).
- (g) Specify with an asterisk (*) whether the INTERVAL MODE is to be LINEAR or LOG(arithmic).
- (h) Perform steps (f)-(j) inclusive in para 5.3.1.
- (j) Press the ROLL key to display Data Entry Form 2 and proceed to para 5.4.2.

5.4.2 *Entering Correlator Parameters (fig 4.7 & 4.8)*

- (a) Perform steps (a)-(f) inclusive in para 5.3.2.
- (b) Refer to para 5.4.3 for the selection of CO-ORDINATES.
- (c) Perform steps (h)-(r) inclusive in para 5.3.2.
- (d) Press the DATA DISPLAY key to display Results Page 1.

Reference Fig 4.8:

- (e) Press the START key to start measurement.
- (f) Refer to para 5.5.
- (g) If results accumulate on more than one page, subsequently pressing the ROLL key causes results pages 1-10 to be displayed consecutively.

CORRELATOR PARAMETERS (SWEEP FREQUENCY MEASUREMENT)

TO DISPLAY THIS FORM : PRESS KEYS

DATA ENTRY

FORM

2

S	T	A	R	T	F	R	E	Q	U	E	N	C	I	0	0	.	5	] H	Z					
F	I	N	A	L	F	R	E	Q	U	E	N	C	I	9	9	9	9	] H	Z					
H	A	R	M	O	N	I	C					C	I											
G	E	N	.	A	M	P	L	I	T	U	D	E		C	5	.	0	0	] V R M S					
G	E	N	.	B	I	A	S					C			0			] V						
C	O	R	R	E	L	A	T	O	R		R	A	N	G	E		A	U	T	O	[*]			
C	H	A	N	N	E	L		A	C	5	0	0	] V		B	C	5	0	0	] V				
I	N	T	E	G	R	A	T	I	O	N			C		1	0		C	Y	C	L	E	S	
D	E	L	A	Y								C		.	2			S	E	C	O	N	D	S
I	N	T	E	R	V	A	L	S					C		1	2								
I	N	T	E	R	V	A	L	M	O	D	E		L	I	N	E	A	R	[*]	L	O	G	[]	
C	H	A	N	N	E	L			A	C	] B	C	*	] B	/	A	C	]						
C	O	-	O	R	D	I	N	A	T	E	S		P	O	L	A	R							
												R	E	A	D	Y								

FIG. 4.7 DATA ENTRY FORM 2

TO DISPLAY THIS PAGE : PRESS

DATA
DISPLAY

										PAGE		1	
N o	F R E Q			A M P L			P H A S E			S 1	S 2		
	H z			V			°			%	%		
1	1	0	0 . 5	5 . 0	0	1 2 3	3	5	9 . 9	. 0	0	. 6	5
2	1	0	0 0 .	4 . 9	9	8 1 2	3	5	9 . 9	. 0	0	. 0	0
3	1	9	0 0 .	4 . 9	9	8 4 7	3	5	9 . 8	. 0	0	. 0	0
4	2	8	0 0 .	5 . 0	0	2 1 6	3	5	9 . 7	. 0	0	0 . 0	
5	3	6	9 9 .	4 . 9	9	9 4 1	3	5	9 . 7	0 . 0		. 0	0
6	4	5	9 9 .	5 . 0	0	1 1 4	3	5	9 . 7	. 0	0	. 0	0
7	5	4	9 9 .	5 . 0	0	2 0 6	3	5	9 . 7	. 0	0	. 0	0
8	6	3	9 9 .	5 . 0	0	1 9 0	3	5	9 . 9	. 0	0	. 0	0
9	7	2	9 9 .	4 . 9	9	9 7 1	3	5	9 . 5	. 0	0	. 0	0
1 0	8	1	9 9 .	4 . 9	9	9 9 3	3	5	9 . 7	0 . 0		. 0	0
1 1	9	0	9 9 .	5 . 0	0	1 1 7	3	5	9 . 7	0 . 0		0 . 0	
1 2	9	9	9 9 .	5 . 0	0	2 4 4	3	5	5 . 3	. 0	0	. 0	0
C H A N N E L				B			M E A S U R E						

FIG. 4.8 RESULTS PAGE (1)

NOTE
GRID LINES SHOWN FOR CLARITY

5.4.3 Selection of CO-ORDINATES

Fig 4.9 shows the labelling of results at the top of the Results Page for each type of co-ordinates and measurement.

- (a) To select cartesian co-ordinates, press the a,b key.
- (b) To select log-polar co-ordinates, press the Log R, ϕ key.
- (c) To select polar co-ordinates, press the R, ϕ key.

5.5 Measurement Sequence

5.5.1 Instrument Status Indicators - Fig 4.10

- (a) Once the START key has been pressed to initiate the measurement cycle, DELAY brights up for the selected delay period before each measurement cycle (when a data entry page is being displayed).
- (b) MEASURE flashes at the bottom of the display during each measurement cycle.
- (c) If the instrument remains in READY status after the START key is pressed and a field indicator (e.g. FREQUENCY, HARMONIC) flashes, this means that the data in this field is incorrect in some way (see para 2.5 above). The cursor is positioned at the m.s.d. of the incorrect field automatically. Entering correct data and pressing the START key again allows the measurement process to begin.
- (d) If measurement ceases and OVERRANGE is indicated, this means that a correlator input greater than 500 V has been received. (If too low a range is selected manually, the instrument ranges up automatically).
- (e) If measurement ceases and UNDERRANGE is indicated, this means that an input of less than 5% of the selected correlator range has been received (less than 0.25% if the 0.05 V range is selected).
- (f) When the required measurement has been completed, the instrument returns to READY status and continues to display the results until switched off or a new measurement is started.
- (g) Measurement can be terminated at any stage by pressing the STOP key. The instrument returns to READY status.
- (h) *PAUSE facility*
 - (i) Measurement can be interrupted at any stage in order to change unprotected parameters (see table 4.1) by pressing the PAUSE key. PAUSE status is now indicated at the bottom of the display.
 - (ii) If a results page is being displayed, press the DATA ENTRY key.
 - (iii) The field indicators of the unprotected parameters bright up.

(CARTESIAN)

N	o		F	R	E	Q		R	E	A	L					I	M	A	G				
				H	z			A					+			j	B						

(LOG - POLAR : RATIO)

N	o		F	R	E	Q		G	A	I	N	d	B			P	H	A	S	E		S	1		S	2
				H	z			L	o	g	R						o					%			%	

(LOG - POLAR : ABS)

N	o		F	R	E	Q		A	M	P	L	d	B			P	H	A	S	E		S	1		S	2
				H	z			L	o	g	V						o					%			%	

(POLAR : RATIO)

N	o		F	R	E	Q		G	A	I	N					P	H	A	S	E		S	1		S	2
				H	z				R								o					%			%	

(POLAR : ABS)

																						P	A	G	E	1
N	o		F	R	E	Q		A	M	P	L					P	H	A	S	E		S	1		S	2
				H	z				V								o					%			%	

FIG. 4. 9 RESULT LABELLING
(SWEEP FREQUENCY MEASUREMENT)

- (iv) If changes are required on the Options Page, press the ROLL key.
- (v) Unprotected parameters can now be changed after positioning the cursor in the appropriate field.
- (vi) Pressing the START key now initiates the new measurement.

R	E	A	D	Y					

O	V	E	R	R	A	N	G	E	

M	E	A	S	U	R	E			

U	N	D	E	R	R	A	N	G	E

P	A	U	S	E					

**FIG. 4. 10 INSTRUMENT STATUS
(BOTTOM OF ALL DISPLAYS)**

5.5.2 *Statistics of Small Magnitude.* In the 3-character statistics result fields values of small magnitude sometimes appear as 0.0 and sometimes as .00. When the third digit would have been 0, the display gives .00. When the third digit would have been greater than 0, then 0.0 is displayed.

6. OPERATIONAL MAINTENANCE

6.1 Input-Output Check

The analyser can be effectively operated and display results without connection to any other equipment. The generator output can be connected directly to a correlator input with an input-output cableform. Parameters can then be entered and results displayed as when measuring the response of an external system.

6.2 PSU Fuses and Indicators

Fig 4.11 shows the locations and ratings of the fuses in the various supplies to the processor, memory, generator and correlators. All d.c. supply fuses and indicator l.e.ds are contained in the PSU compartment. For access to these, proceed as follows:

————— WARNING —————

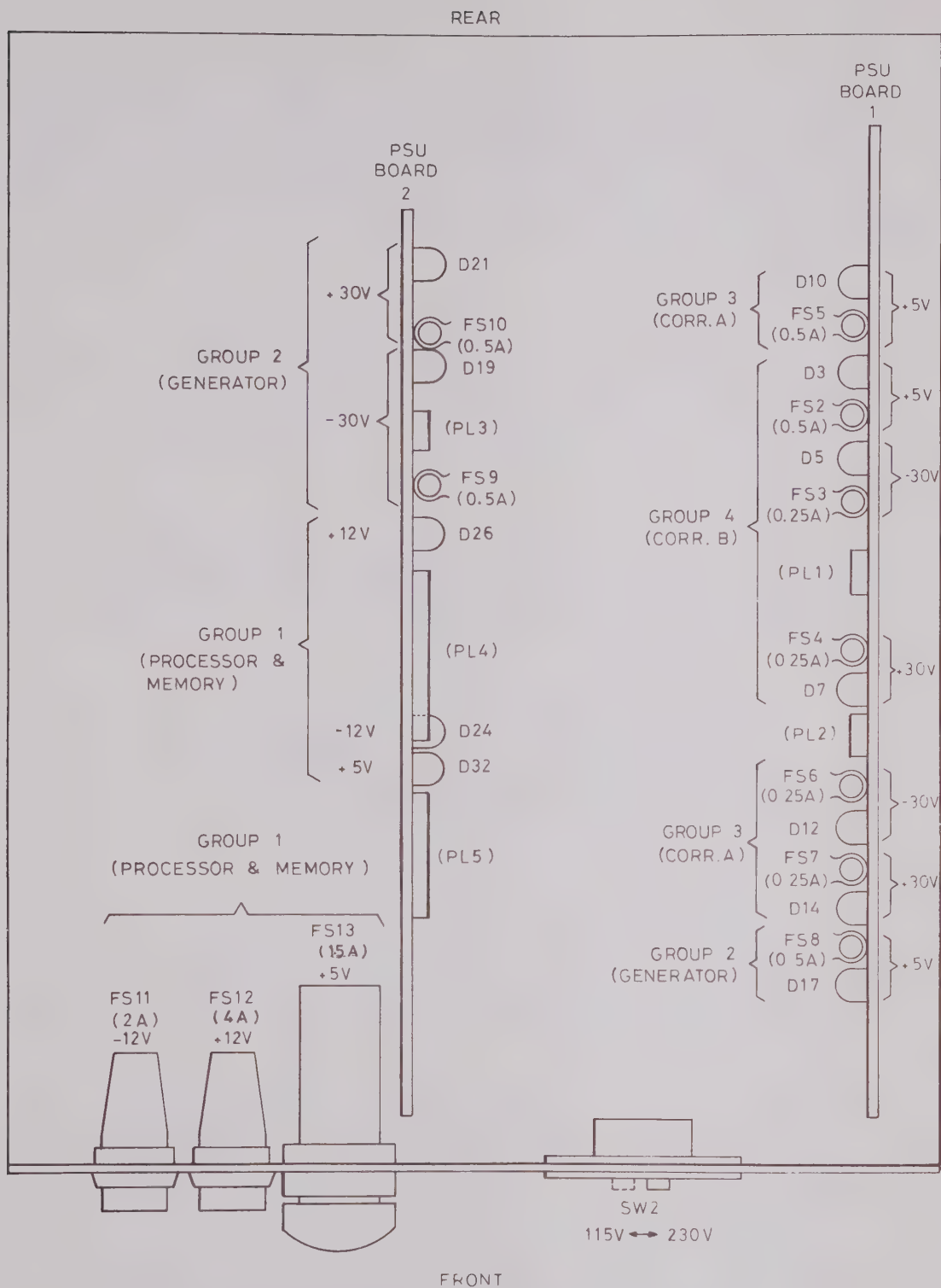
VERY HIGH VOLTAGES are present inside the instrument cabinet while power is switched on and for a period after switching off. The EHT for the display is generated in the area just in front of the PSU compartment.

MAINS VOLTAGE is present inside the PSU compartment while power is switched on.

- (a) Loosen the 2 screw fasteners; 1 behind the keyboard (accessed by pulling the keyboard forward from the bottom) and 1 at the top centre of the back panel.
- (b) Lift off the top cover. All the supply indicator lamps can now be seen through the clear cover on the PSU compartment (the left rear compartment of the cabinet).
- (c) Fuses FS11, FS12 and FS13 can be changed after switching power off and taking precautions to guard against any residual EHT.
- (d) For access to fuses FS2-FS10 inclusive, the PSU compartment cover must be removed by removing its 4 corner screws. Switch power off before removing fuses.

6.3 Preset Display Controls

The display controls which should rarely require adjustment (line hold, frame hold and height) are potentiometers mounted on a circuit board inside the cabinet (see fig 4.12). For access to these controls remove the top cover of the cabinet as in para 6.2 above, taking note of the high voltage warning.



THIS DIAGRAM WAS DERIVED FROM:
DWG. ISSUE

E82070	2
D82071	1
D82076	1
E81221 SHEET 2	2

MAINS FUSE FS1
(BACK PANEL)

230V : 2A
115V : 4A

FIG. 4.11 PSU FUSE AND INDICATOR LOCATIONS

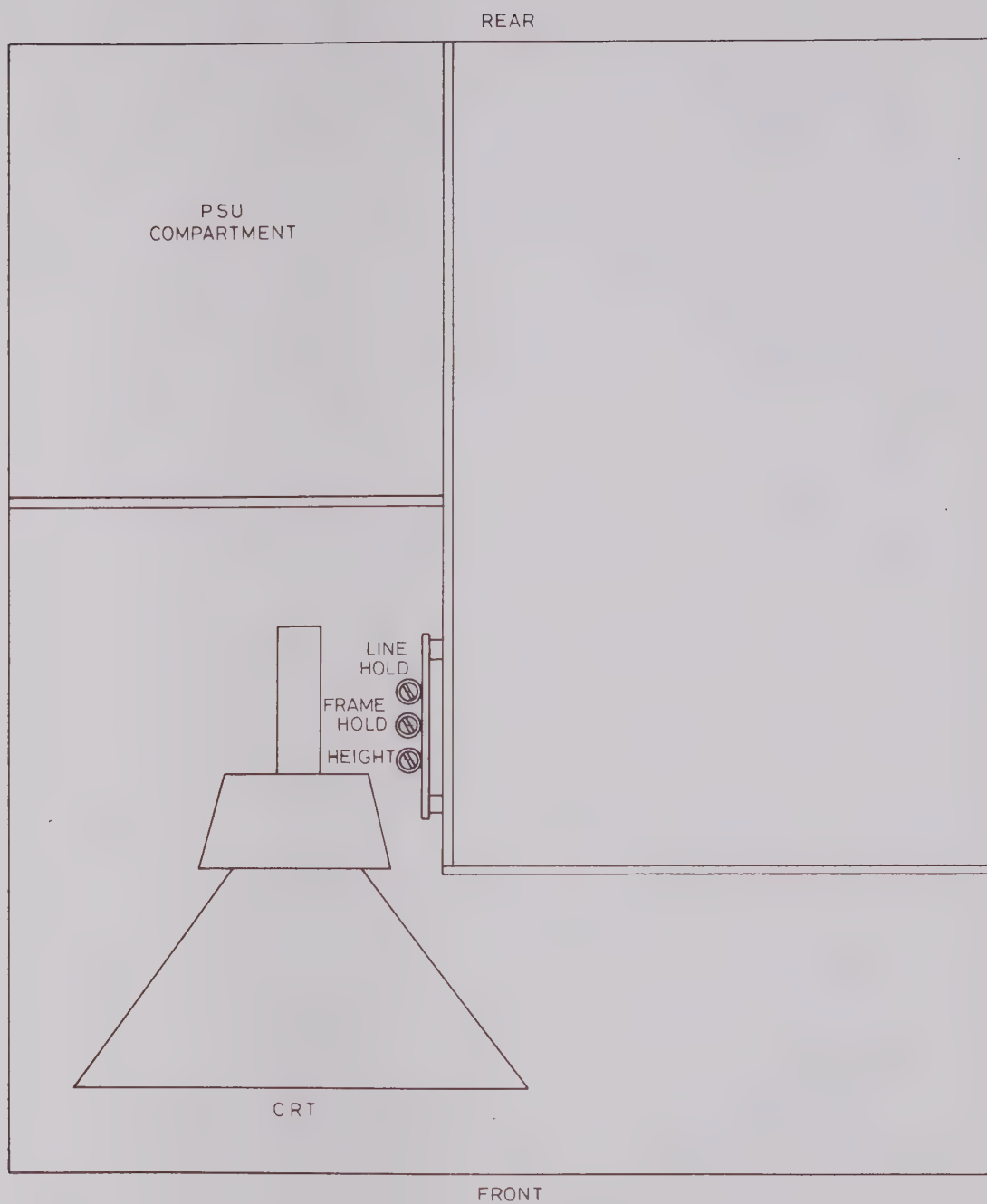


FIG. 4.12 PRESET DISPLAY CONTROL LOCATIONS

SECTION 5
THE FRA SYSTEM

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Introduction

In order to understand how the F.R.A. achieves its purpose, not only is it necessary to understand how the system hardware functions, but it is also essential to have a clear appreciation of the sequence of operations performed by the hardware, and of how this sequence and the individual operations may be influenced by the Operator and/or the system software. The basic sequence of operations performed by the hardware, Operator and software under typical test conditions is illustrated in the flow chart of fig. 5.1.1; the actions performed during this sequence are outlined below.

DESCRIPTION

Data Entry Phase (Steps 01 to 07)

When power is first applied to the F.R.A., the software initialises the system to a condition in which the generator and correlator parameters and options are selected in accordance with the default values listed in table 4.1, and Data Entry Form 1 with Ready status set is called up for display.

Following the short warm-up period required by the c.r.t., the initialised display is presented to the Operator. Using the keyboard, the Operator can now adjust the parameters and select the options as appropriate to the test being performed, each new value or selection being displayed as it is entered.

When all the relevant data has been entered, the Operator presses the START key to initiate the measurement phase of the sequence. However, before allowing measurement to proceed, the software examines the parameter values and option selections for correct format, completeness, etc. Should an error be found, further progress through the sequence is inhibited and the software draws the Operator's attention to the incorrect entry by causing the appropriate field to flash. After correcting the error, the Operator must again press the START key if he still wishes the test to be performed.

Measurement Phase (Steps 08 to 13)

The measurement phase is performed automatically, although the Operator may intervene at any time by pressing the PAUSE key or the STOP key. If the PAUSE key is used, the measurement is interrupted and the software causes Pause status to be indicated. The Operator can then alter any parameter or option specified in table 4.1 as being unprotected, the software aiding the Operator by causing those fields of the Data Entry Form and Option Page containing such parameters to flash. The new measurement is initiated by pressing the START key, as before. When the STOP key is used, measurement is halted unconditionally and the F.R.A. reverts to Ready status.

The first action of the phase is to adjust, under software control, the generator and correlator circuits as required to set up the test conditions demanded during the data entry phase and to make available the generator output signal. The system and the unit under test are then allowed to settle for the period specified in the delay field of the Data Entry Form, the software causing Delay status to be indicated during the period.

The actual measurement begins with an examination by the software of the options data, to ascertain whether manual or auto bias rejection has been demanded. If manual bias rejection is indicated, then the correlate mode is entered. When, however, auto bias rejection is required, the software next examines the generator frequency data field. If that examination shows that the requested frequency is greater than 10 Hz, the correlator enters the d.c. averaging mode. If the requested frequency is 10 Hz or less, the software diagnoses an incorrect entry (auto bias rejection can only be used at output frequencies above 10 Hz in early versions of software) and duly returns the F.R.A. to Ready Status and indicates the error as previously described.

In the correlate mode, the hardware samples the output from the item under test at a rate of 48 kHz and processes each sample so as to obtain a pair of products representing instantaneous values of the sine and cosine waves at the measurement harmonic frequency (see section 2.3). Successive products of each quantity are summed until 256 samples have been taken and the accumulated products are then written to memory under hardware interrupt control. The sampling, processing, accumulation and storage actions continue for a period equivalent to the time required to perform the number of generator output cycles specified in the integration cycles field of the Data Entry Form.

To enable the boundaries of each block of samples to be determined, the hardware keeps a count (up to 256) of the number of samples taken, the occurrence of each count of 256 initiating the interrupt action and also resetting the count to zero. However, depending upon the measurement harmonic frequency and number of integration cycles selected, so the correlation period may not divide into an exact number of blocks. When this is so, the software calculates the number of samples which must be processed prior to the first interrupt to ensure that the completion of the required number of integration cycles coincides with the completion of a sample block, and presets the counter so that the first count of 256 occurs when that number of samples has been taken.

The correlator remains in the d.c. averaging mode for a period of 100 ms + the time required to complete one cycle at the generator output frequency. During this time, the incoming signal is sampled, and the results of processing accumulated and read out, in an identical manner to that used in the correlate mode. However, instead of the processing taking the form of effectively multiplying the samples by a sine and a cosine wave, it now consists of multiplying the samples by a constant. If the samples are uniformly disposed about the zero volt line, then their sum over a complete cycle of the F.R.A. input signal is zero. If, however, there is a d.c. displacement of the signal, then the sum is not zero, and its magnitude indicates the size of the displacement and its sign the direction. Using this information, the software can calculate the value and sign of the d.c. bias which

must be injected into the input signal to counteract the displacement, and adjust the correlator parameters accordingly before allowing it to enter the correlate mode.

Throughout the phase, the software causes the Measure status indicator to flash during each measurement. If an overrange condition is detected at any time, the software causes the instrument to range up until a suitable measurement range is reached; if, however, the condition persists when the 500V range is selected, then the software halts the measurement and advises the Operator by instructing the hardware to display Overrange status. When an input amplitude of less than 5 per cent of the selected range (less than 0.25 per cent if the 0.05V range is selected) is received, the software diagnoses this as an underrange condition, stops the measurement and causes Underrange status to be indicated.

Results Phase (Steps 14 to 17)

With all of the measurement results in memory, the software commences to manipulate them as required to enable them to be displayed in the format specified in the Data Entry Form and Options Page. The types of computation leading to the various results obtainable are shown in fig. 2.2.

If the system is operating in the single frequency mode, then if the last display selection made by the Operator was the Data Entry Form, on completion of results processing the Form is automatically replaced by Results Page 1; if the last display selection was the Options Page, that Page will continue to be displayed until the DATA ENTRY key is pressed, whereupon Results Page 1 is displayed. If the system is operating in the swept frequency mode, the DATA DISPLAY key must be operated to obtain Results Page 1. Further Results Pages are obtained by use of the ROLL key.

To obtain statistical results, it is necessary to repeat the measurement and results processing a number of times. To facilitate this, a repeat facility is included. On completion of the results processing, the software examines the fields of the input data to determine whether a repeat is required and, if so, whether the number of measurements specified by the Operator have been performed. Should the results of this examination indicate that further measurement is required, the system is automatically returned to the start of the measurement phase.

If the repeat mode has not been called up, the results of the current measurement remain on display until either the Operator presses the START key to initiate a further measurement under the same test conditions, until he calls up a Data Entry Form or Options Page to enter data for a new test, or until power is removed from the system.

Phase Stop

The phase stop facility enables measurement to be commenced at one of the cardinal points of the generator output cycle. To make such a measurement, the Operator first proceeds to initiate a 'normal' measurement as described above, the only proviso being that manual correlator ranging must be selected. On completion of this measurement (which serves to detect any errors and to set up the generator and

corrélator, and the results of which are ignored), he uses the SHIFT and numeric keys to enter the phase angle at which he wishes measurement begin, as follows:

SHIFT, 0 = 0°
SHIFT, 1 = 90°
SHIFT, 2 = 180°
SHIFT, 3 = 270°

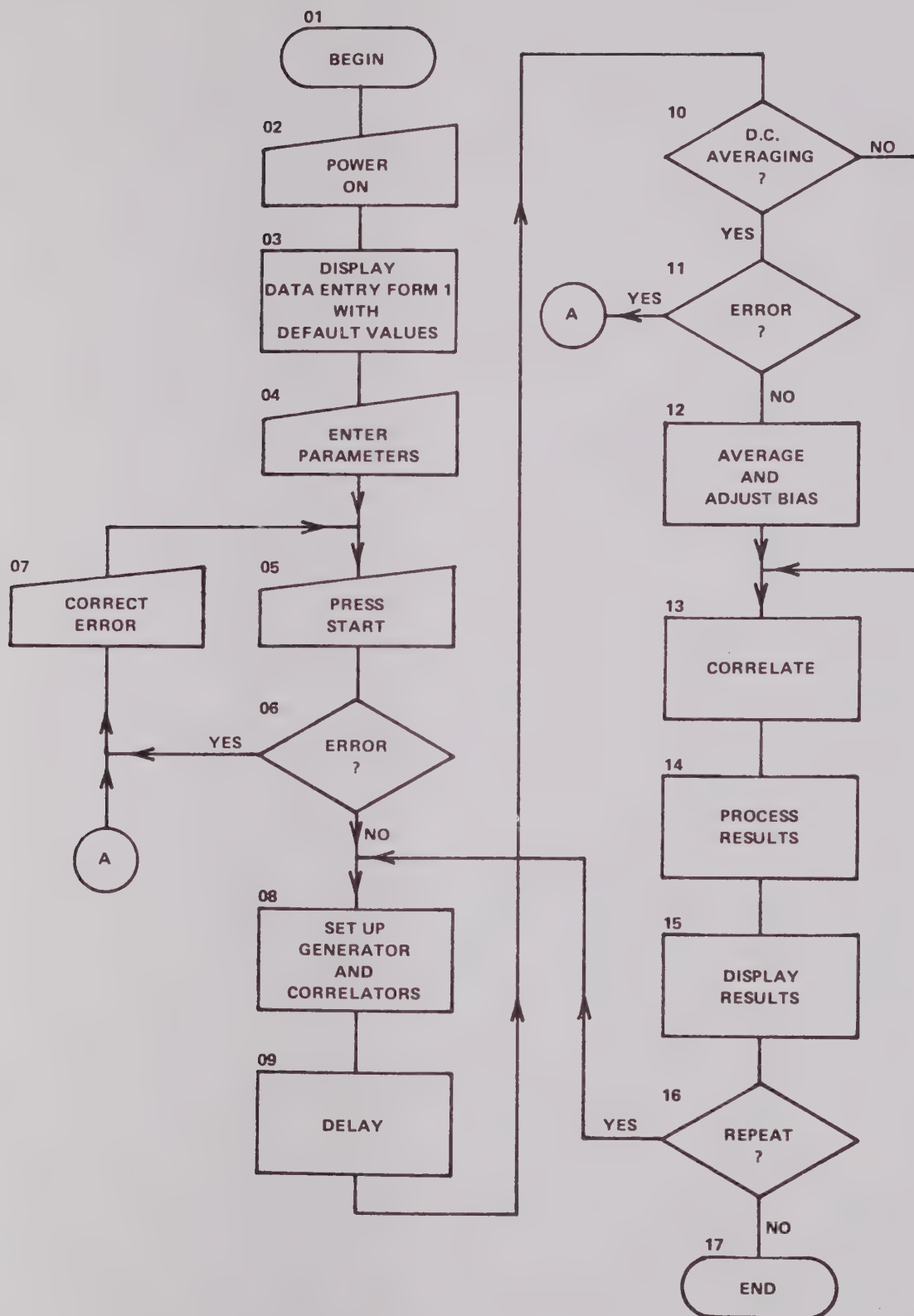


FIG 5.1.1 SEQUENCE OF OPERATION

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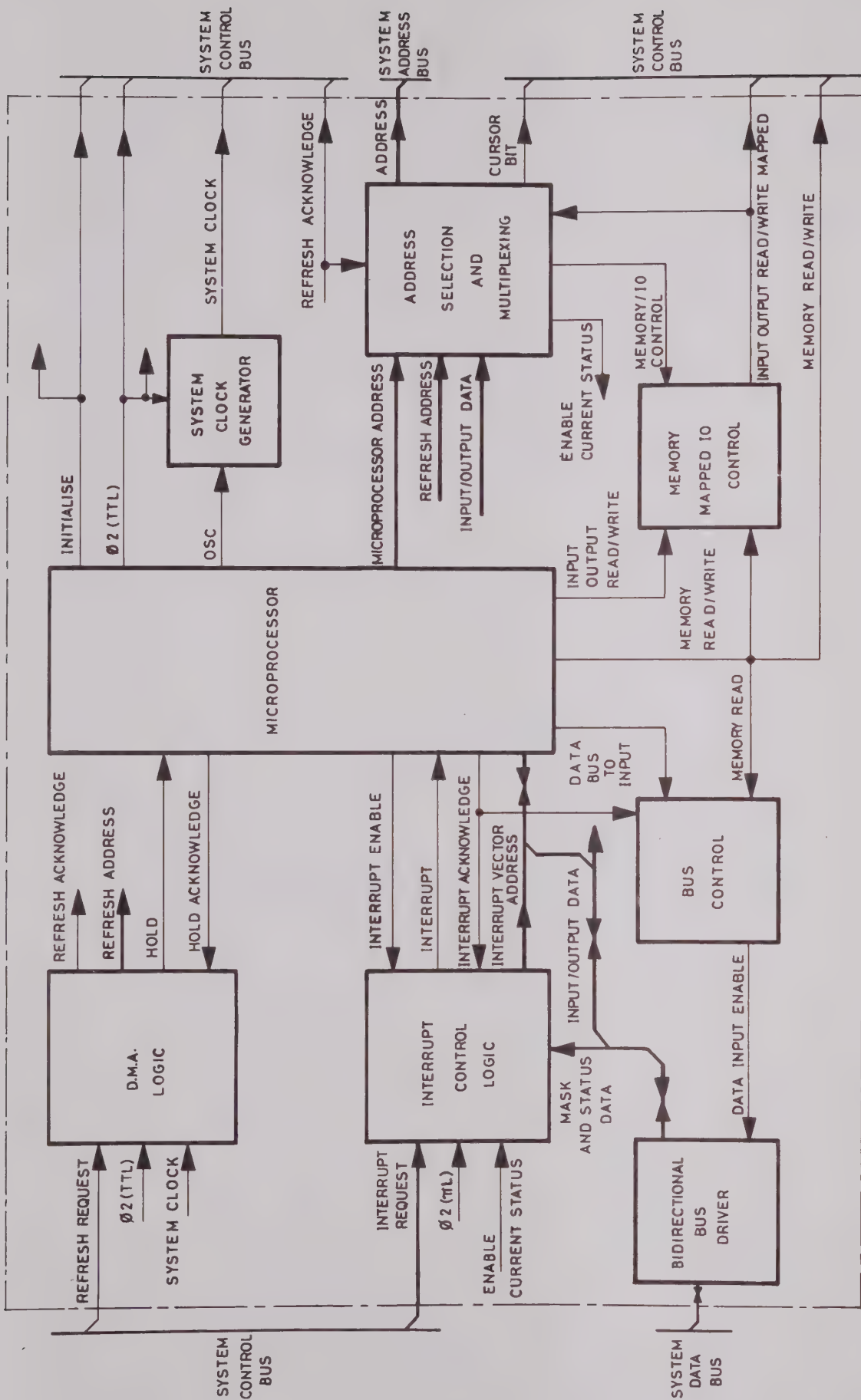


FIG 5.2.1. MICROPROCESSOR

INTRODUCTION

The Frequency Response Analyser is implemented as a microcomputer system configured as shown in fig. 5.2.7. The purpose and operation of each of the main system elements indicated in the diagram are described in the subsections which follow. The physical location of each of the assemblies which make up these elements is illustrated in fig. 5.2.8.

MICROPROCESSOR

The Microprocessor (fig. 5.2.1) is the heart of the F.R.A. system, controlling the sequence of operations performed, the Display, and a considerable proportion of the arithmetic processing.

Microprocessor

The Microprocessor itself consists of three integrated-circuit packages - a clock generator and driver, a processor, and a system controller and data bus driver - together with a number of directly-associated logic elements and circuit components.

The crystal-controlled clock generator and driver provides the clocking arrangement required by the processor, and also a number of auxiliary functions and timing signals used throughout the system.

The processor package contains a complete, 8-bit parallel, central processing unit. Separate 16-bit address and 8-bit bidirectional data busses are used to facilitate interfacing with the Memory and other peripheral devices. Provision is made for a direct memory access (D.M.A.) mode of working.

The system controller and data bus driver generates all the control signals required to directly interface the processor with the peripherals, and also provides buffering between the System Data Bus and the processor data bus.

System Clock

A crystal-frequency output (OSC.) from the Microprocessor is operated upon by the System Clock Generator in such a manner as to obtain a SYSTEM CLOCK signal which is at 6.144 MHz (one third of the crystal frequency) and which is in synchronism with the $\Phi 2$ (TTL) clock output from the Microprocessor.

Memory Read and Write

A memory read commences with the Microprocessor placing on its address bus the address of the memory location at which the read is to be performed, this being transmitted to the Memory via the Address Selection and Multiplexing circuits and the System Address Bus. Shortly after, the Microprocessor issues a DATA BUS TO INPUT command to the Bus Control, followed by a MEMORY READ command to both the Bus Control and the Memory; also, it sets its internal data bus to the input condition to allow the incoming data or instruction to enter the processor. The inputs to the Bus Control cause that circuit to generate DATA INPUT ENABLE, setting the Bidirectional Bus Driver to the input

mode and hence enabling the contents of the System Data Bus to be input to the Microprocessor.

When an instruction requires the Microprocessor to perform a memory write operation, the first action of the sequence is to transmit the write address to the Memory via the same path as is used during a memory read. The Microprocessor then issues a MEMORY WRITE command to the Memory. No DATA INPUT ENABLE is generated during a write, and the internal data busses are set to the output condition. Hence the data output by the Microprocessor during the cycle passes via the Bidirectional Bus Driver to the System Data Bus, and so to the Memory.

Input Output Read and Write

If the Microprocessor wishes to read data from, or write data to, a peripheral other than the Memory, it uses similar sequences of operation to those used to read from, or write to, Memory. In such instances, however, the address sent to the System Address Bus is the vector and port address of the peripheral device involved in the transaction (see appendix A); also, an INPUT OUTPUT READ or INPUT OUTPUT WRITE signal is generated. The Memory Mapped IO Control gates the INPUT OUTPUT signal with the corresponding MEMORY signal and the most significant address bit. If both the latter are also true, INPUT OUTPUT READ MAPPED or INPUT OUTPUT WRITE MAPPED, as appropriate, is sent to the peripheral via the System Control Bus. In the case of a read, INPUT OUTPUT READ MAPPED is also used to cause the Bidirectional Bus Driver to be set to the receive mode.

Interrupts

When instructed to enable interrupts, the Microprocessor enables the Interrupt Control Logic and writes the current 'mask' and 'status' information to it. The 'mask' information effectively defines which of the eight possible interrupt levels with access to the Logic is to be allowed to interrupt the Microprocessor. The 'status' information defines the basis upon which interrupts are to be serviced, i.e. if the highest priority request present is to be serviced regardless of its level, or only when it is of a higher priority level than that indicated by the 'mask'.

All incoming INTERRUPT REQUESTS are first priority-encoded and tested for validity against the mask. Providing that an interrupt is not in progress and a valid request is detected, the Interrupt Control Logic then sends INTERRUPT to the Microprocessor.

On completion of the current instruction, the Microprocessor acknowledges the request. The Interrupt Control Logic responds to the acknowledgement by outputting to the Microprocessor the interrupt vector address for the highest priority valid request present, causing the Microprocessor to commence operations at the appropriate Restart. The return to the main program is under software control.

When it accepts the interrupt, the Microprocessor removes INTERRUPT ENABLE, thus preventing the Control Logic from requesting further interrupt action. On entering the service routine, it restores the enable signal and any request of a higher priority than that which initiated the current interrupt can now be serviced.

Direct Memory Access

Like interrupt requests, D.M.A. requests are first priority-encoded and then serviced in order of priority. However, although the circuit provides for three request inputs to the DMA Logic, only that associated with refreshing the Display and the Memory is used in the present application. Thus only the sequence of events initiated by a refresh request is described here.

Following receipt of REFRESH REQUEST, the D.M.A. Logic generates a HOLD input to the Microprocessor. As soon as the latter has completed the current machine cycle, it enters the 'hold' state, sends HOLD ACKNOWLEDGE to the D.M.A. Logic, 'floats' its address lines, and isolates its data bus from the System Data Bus. The Logic responds to this acknowledgement by outputting a REFRESH ACKNOWLEDGE signal of some 200 ns duration to the Address Selection and Multiplexing circuits and to the System Control Bus, resulting in the REFRESH ADDRESS being passed to the Address Selection and Multiplexing circuits, a read being initiated at the Memory, and the REFRESH REQUEST being withdrawn. Shortly after the trailing edge of REFRESH ACKNOWLEDGE, the D.M.A. Logic ceases to generate HOLD, causing the Microprocessor to terminate HOLD ACKNOWLEDGE. The D.M.A. thus returns to the quiescent condition and normal Microprocessor working resumes.

Address Selection and Multiplexing

The Address Selection and Multiplexing circuit constantly monitors the Microprocessor address lines to determine whether the current address is:

- (a) the Interrupt Control Logic Address,
- (b) a refresh address, or
- (c) the cursor bit address.

If it is found to be the Interrupt Control Logic address, then during INPUT OUTPUT WRITE MAPPED the circuit applies ENABLE CURRENT STATUS to the Logic to load the 'mask' and 'status' information.

When a refresh address is detected, REFRESH ADDRESS is combined with the page address set by program and currently held in the circuit, and the resultant address transmitted to Memory via the System Address Bus to define the address at which the D.M.A. read is to be performed.

If the cursor bit address is found, the circuit generates CURSOR BIT, which then passes to the Display via the System Control Bus.

Power-on Reset

When power is first applied to the system, the Microprocessor generates an INITIALISE pulse which clears various devices throughout the system.

MEMORY

The Memory (fig 5.2.2), depending upon the type of memory board fitted, provides up to either 24,576 (earlier models) or 49,152 words (Memory 2 board fitted) of 8-bit length. 16,384 words (early models) or 32,768 (Memory 2) of this storage can be in the form of programmable read only

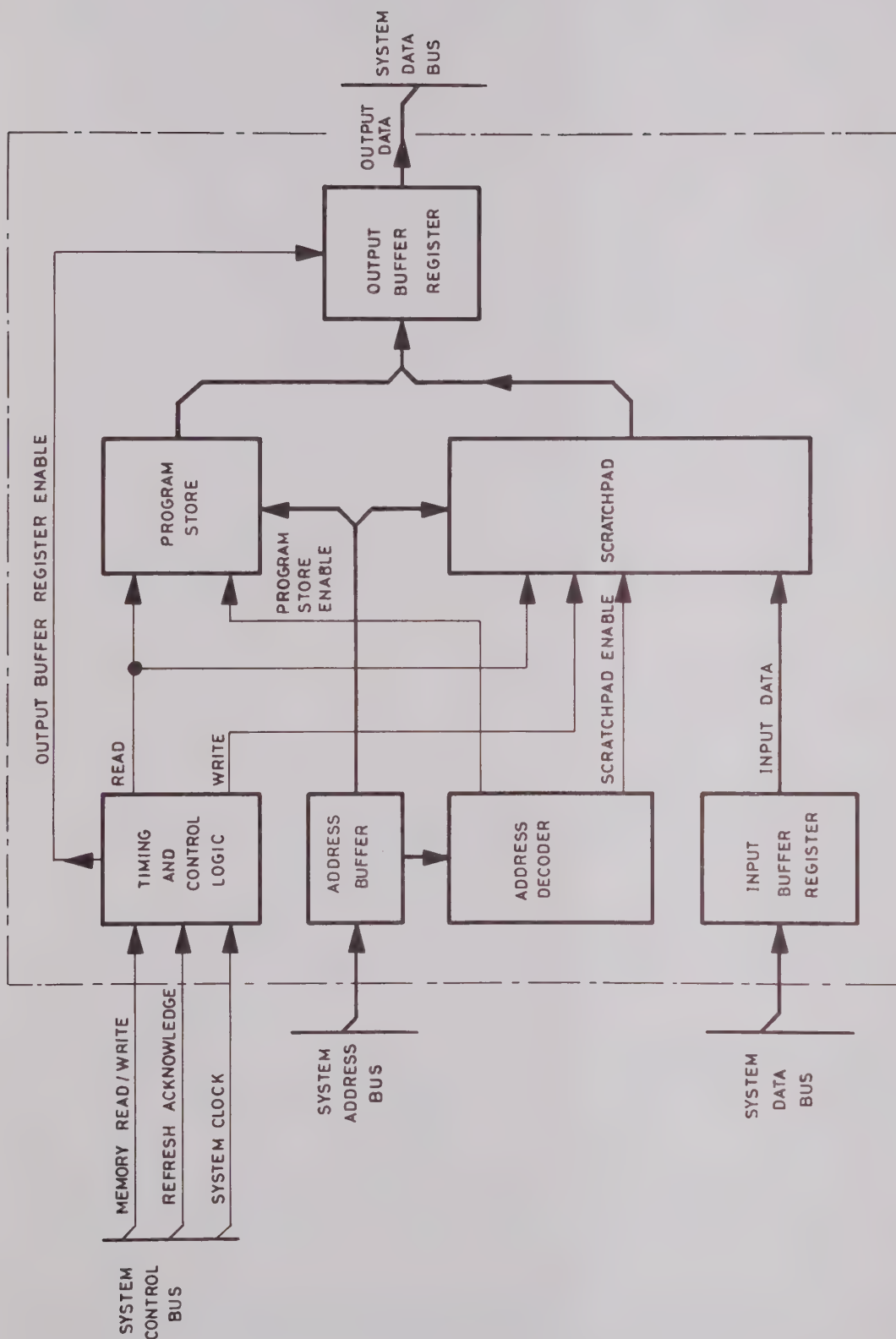


FIG 5.2.2. MEMORY

memory, used to hold the F.R.A. control operations program; the remaining 8,192 words (earlier models) or 16,384 words (Memory 2) are in the form of random access memory, used as a scratchpad for calculations, stacks, results, and display data. Overall control of the function is exercised by the Microprocessor, via the Timing and Control Logic.

To perform a memory read, the Microprocessor first places on the System Address Bus the address of the memory location at which the operation is to be performed. The Address Decoder examines the state of the m.s.b. of this address to determine which of the two areas of storage is to be used during the operation (bit low = Program Store; bit high = Scratchpad) and enables the required address in the appropriate store area.

Shortly after issuing the address, the Microprocessor requests the memory read via the System Control Bus. This causes a READ command to be passed to both the Program Store and the Scratchpad, and the Output Buffer Register to be enabled. Thus the data from the addressed location appears on the System Data Bus.

The control sequence for a memory write operation is similar to that used during a memory read; however, since the Program Store is a read only store, the WRITE command is passed to the Scratchpad only. The data which is to be written to the pad appears on the System Data Bus coincident with the memory write request.

The Scratchpad is a dynamic store and must be refreshed by reading at 2 ms intervals. As it is also necessary to refresh the display data within the same period, the two operations have been combined. Thus each time a request to refresh the display is acknowledged, a scratchpad read is initiated.

GENERATOR

The function of the Generator (fig. 5.2.3) is to generate an analogue GENERATOR OUTPUT signal which possesses the frequency, waveshape, amplitude, phase and d.c. offset characteristics input by the Operator via the Keyboard.

Interfacing

The Generator interfaces with the System Data Bus via the eight, write only, interface registers indicated in fig. 5.2.3 and described in appendix A. The Address Decoder constantly monitors the System Address Bus bits. When the value of the address bits equals that of the vector and port address allocated to one of the interface registers, the arrival from the Microprocessor of an INPUT OUTPUT WRITE MAPPED pulse causes the contents of the System Data Bus to be strobed into the appropriate register and hence to be applied to the area of the generator circuits which they influence.

Development of Generator Output

In the Phase Locked Loop, the accurate, 1024 Hz output of the Reference Frequency Generator is multiplied by the contents of the Frequency Mantissa Interface Registers. The result of this operation is then divided by 2^n , where n is the number held in the Frequency Exponent

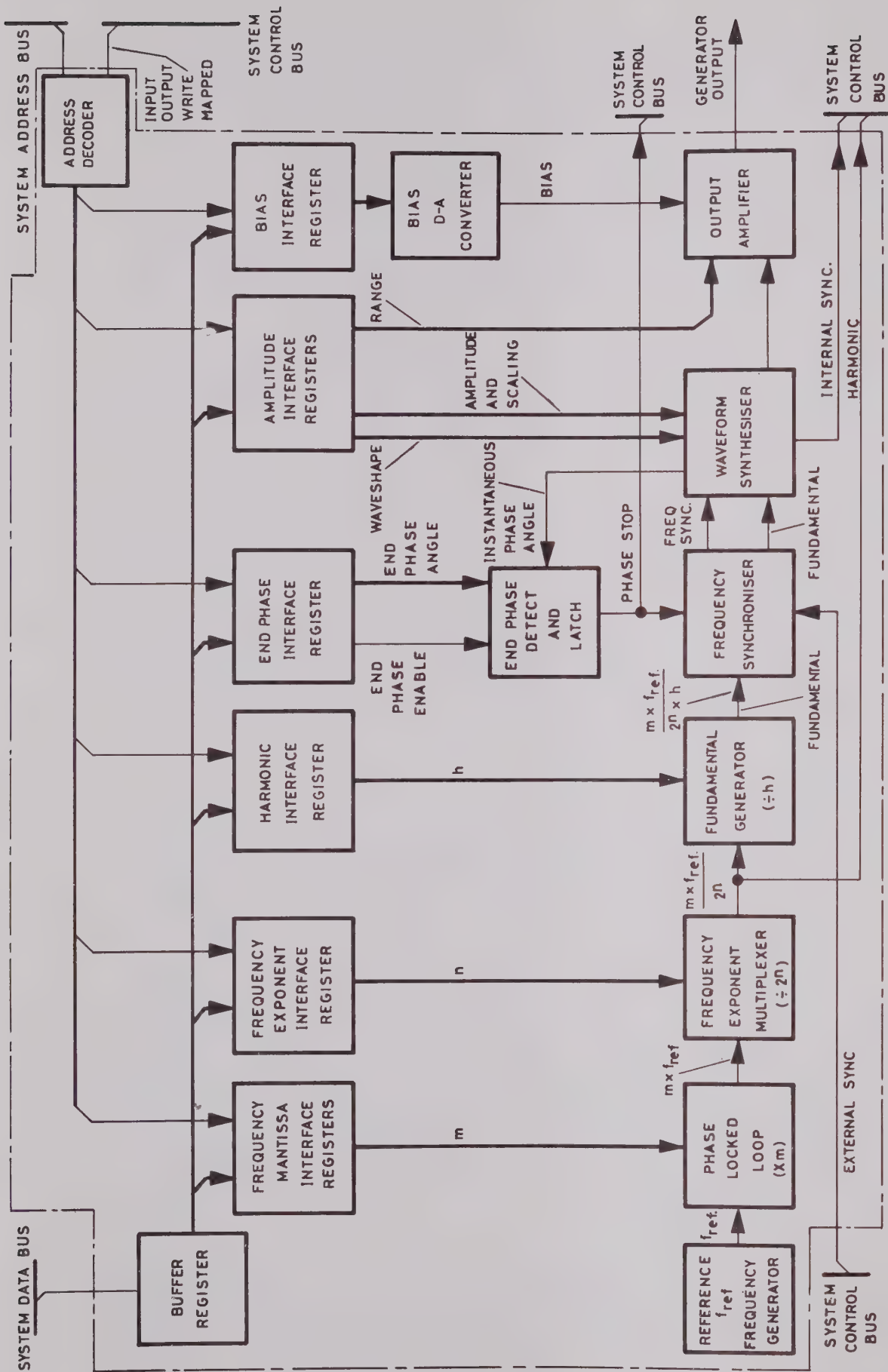


FIG 5.2.3. GENERATOR

Register, to produce the digital HARMONIC signal at 1024 times the harmonic frequency at which analysis is to be performed.

The HARMONIC signal passes via the System Data Bus to the Correlator, where it is used in the analysis process, and to the input of the Fundamental Generator. In the latter, it is divided by the harmonic number contained in the Harmonic Interface Register, resulting in a digital FUNDAMENTAL signal at 1024 times the required output frequency.

The Frequency Synchroniser applies FUNDAMENTAL to the signal input of the Waveform Synthesiser circuits. There a count of the incoming pulses is kept and used to define the instantaneous phase of the GENERATOR OUTPUT, which therefore advances in steps of $\frac{360^\circ}{1024}$ ($\approx 0.35^\circ$).

During the 'internal' mode of frequency synchronisation, this count is allowed to proceed cyclically. If, however, the 'external' mode is used, then on each leading edge of the EXTERNAL SYNC. signal the Synchroniser outputs a FREQUENCY SYNC. pulse to the Synthesiser which resets the count to zero; hence the start of each cycle of GENERATOR OUTPUT is always referred to the same point in the EXTERNAL SYNC. signal.

Using the phase information extracted from the FUNDAMENTAL signal and the WAVESHAPE, AMPLITUDE and SCALING information contained in the Amplitude Interface Registers, the Waveform Synthesiser now proceeds to generate an analogue signal which is of the desired shape (sine wave, square wave or triangular wave) and which, after further processing in the Output Amplifier, will result in the GENERATOR OUTPUT being at the required amplitude (within the overall range 0.001V to 9.99V) appropriately scaled r.m.s. or peak.

In addition to adjusting the amplitude of the Waveform Synthesiser output in accordance with the RANGE data obtained from the Amplitude Interface Registers, the analogue Output Amplifier also makes provision for injecting a d.c. bias into the GENERATOR OUTPUT signal. The value of this bias is held in the Bias Interface Register, and the bias potential is derived from this value by means of a digital-to-analogue converter stage.

End Phase Facility

The end phase facility enables the GENERATOR OUTPUT to be 'frozen' at a phase angle of 0° , 90° , 180° or 270° , as required by the Operator. Whether or not the facility is enabled and the phase angle at which it is to be effective are indicated by the contents of the End Phase Interface Register. The END PHASE ANGLE is continually compared with the INSTANTANEOUS PHASE ANGLE generated by the Waveform Synthesiser. When the two values are equal, and providing the facility is enabled, a PHASE STOP signal is input to the Frequency Synchroniser and the Correlator. The former responds to the signal by removing the FUNDAMENTAL input from the Waveform Synthesiser, thus halting the phase count and hence holding the GENERATOR OUTPUT at a constant phase angle.

To allow normal working to resume, the END PHASE ENABLE signal is removed. If an EXTERNAL SYNC. signal is present, the GENERATOR OUTPUT is then automatically resynchronised to that signal.

CORRELATOR

The function of the Correlator is to sample the F.R.A. analogue input from the item under test at the required rate, to convert each of the samples into an equivalent, serial, digital data word, and to correlate this word to the F.R.A. output signal. Each correlator channel performs this function upon its respective input signal completely independently.

The two correlator channels are identical in configuration and operation and thus only one is described here.

Interfacing

The channel interfaces with the System Data Bus by means of a Bidirectional Bus Driver and the nine interface registers indicated in fig. 5.2.4 and described in Chapter 5.3.

The Address Decoder constantly monitors the System Address Bus bits. When the value of the address bits equals that of the vector and port address allocated to one of the interface registers, the Decoder generates an INTERFACE REGISTER SELECT signal to that register. During the SELECT signal, the arrival of an INPUT OUTPUT READ MAPPED or INPUT OUTPUT WRITE MAPPED pulse - as appropriate to the interface register type - initiates a transfer of data between the selected register and the System Data Bus.

The Bidirectional Bus Driver is normally in the 'receive' mode, allowing data to be written to the interface registers. During read operations, INPUT OUTPUT READ MAPPED is used to switch the Driver to the 'transmit' mode, thus allowing data to pass from the register involved to the System Data Bus.

Input Sampling

The CORRELATOR INPUT signal is applied to an analogue Input Amplifier, where the signal amplitude is adjusted in accordance the measurement RANGE (50 mV, 500 mV, 5V, 50V or 500V) and SCALING (r.m.s. or peak) demanded by the contents of the Command (Write) Interface Register. The Amplifier also makes provision for the removal of any d.c. offset which the signal might contain, this being achieved by injecting into the signal path a d.c. bias of the value and sign specified in the Input Offset Interface Registers.

At the input of the Sampling and Conversion Logic, the ranged and scaled analogue signal is sampled at 20.83 μ s intervals (a rate of 48 kHz) under the control of the SYSTEM CLOCK. The sample is then converted into an equivalent, sign + magnitude, serial digital word, which is stored in the Logic for the remainder of the inter-sample period. All further processing of the digitised sample is performed under the control of the Sampling and Conversion Logic, which generates the appropriately-timed STROBE and CLEAR signals required.

Multiplier

The exact form the next stage of processing takes depends upon whether the CORRELATE mode or the AVERAGE mode of Multiplier working is demanded. If the CORRELATE mode, then two SERIAL PRODUCTS are produced -

one during the first half of the inter-sample period and one during the second half - which represent the magnitude component of the digitised sample (SERIAL MULTIPLICAND) effectively multiplied by a cosine wave and a sine wave, respectively, at the measurement harmonic frequency.

To generate the cosine and sine waves, a count is kept of the HARMONIC CLOCK input from the Generator (1024 times the measurement harmonic). As each analogue signal sample is taken, the Multiplier ascertains the instantaneous phase angle by sampling this count. After a short delay to enable the Sampling and Conversion Logic to derive the SERIAL MULTIPLICAND, the Multiplier generates a digital word representing the cosine of the instantaneous phase angle with which it multiplies the SERIAL MULTIPLICAND, the result of this operation being the SERIAL PRODUCT. At the start of the second half of the inter-sample period, a STROBE input from the Sampling and Conversion Logic causes the Multiplier to generate a digital word representing the sine of the instantaneous phase angle. A second multiplication of the SERIAL MULTIPLICAND then takes place, producing a second SERIAL PRODUCT. The operations described are synchronised with the GENERATOR OUTPUT signal by INTERNAL SYNC., which causes the phase angle counter to be reset to zero at the start of each cycle of the output signal.

When the AVERAGE mode of working is in being, the phase angle counter is not sampled. This results in SERIAL MULTIPLICAND being multiplied by a constant instead of a cosine or sine wave. If the analogue signal samples are uniformly disposed about the zero volt level, then the sum of the SERIAL PRODUCTS over a complete cycle of the channel input signal is zero. If, however, there is a d.c. displacement of the signal applied to the Sampling and Conversion Logic, the sum is not zero and its magnitude indicates the size of the displacement. The Microprocessor can thus calculate the value of the displacement and cause a compensating offset to be applied in the Input Amplifier.

In addition to its use in the above operations, the phase angle count is also suitably decoded to obtain an indication of the sign of the quadrant in which the current instantaneous phase angle is contained.

Production of Common Sum

The SERIAL PRODUCT and QUADRANT SIGN outputs from the Multiplier are passed to the Common Sum Logic. There, each SERIAL PRODUCT is first signed as indicated by the comparative polarity of the SAMPLE SIGN and QUADRANT SIGN information and then added to the appropriate sum of the results of previous sample processing (COS SUM or SINE SUM from the Accumulator). The new cos and sine sums are input to the Accumulator as COMMON SUM, accompanied by appropriately-timed COS STROBE and SINE STROBE signals.

Accumulation and Output of Results

At the Accumulator, successive COMMON SUM, serial digital words are loaded into the appropriate area of temporary storage under the control of the strobe signals, causing the new COS SUM and SINE SUM to appear at the inputs to the Products Interface Registers and to be returned to the Common Sum Logic. This action continues until the number of samples taken equals that specified in the Fraction Interface Register. When this occurs, the Register generates an OUTPUT LATCH pulse which

loads the COS SUM and SINE SUM into their respective registers and, providing that interrupts are enabled, causes an INTERRUPT REQUEST to be raised. On the trailing edge of OUTPUT LATCH, the Accumulator is cleared by RESET in readiness for the next set of products.

When the Microprocessor acknowledges the interrupt, the request is cleared. The Microprocessor then proceeds to read the contents of the Cos and Sine Products Interface Registers.

The Fraction Interface Register takes the form of a 0 to 256, pre-settable counter which is incremented by the SAMPLE STROBE from the Sampling and Conversion Logic each time a sample is taken. Normally, no preset count is loaded and so each read of the Products Registers extracts the data relating to 256 samples, this data then being added to any previously read products until the specified number of cycles of the generator output have been sampled. In many cases, however, blocks of 256 samples will not exactly cover the required number of cycles. When this is so, the Microprocessor presets the Fraction Register so that less than 256 samples are accumulated in the first block.

Overflow

Overflow is detected by suitably decoding the output of the analogue-to-digital converter contained in the Sampling and Conversion Logic. When eight overflow conditions are detected during any one set of samples, an OVERFLOW indication is sent to the Command (Read) Interface Register. The indication is cleared simultaneous with the Accumulator.

Done Indication

Coincident with each INTERRUPT REQUEST, the Interrupt Logic outputs DONE to the Command (Read) Interface Register. The signal is removed when read out of the m.s. byte of the Cos Products Interface Register is completed. Thus DONE indicates that the Correlator has raised an interrupt request but that this request has not yet been serviced.

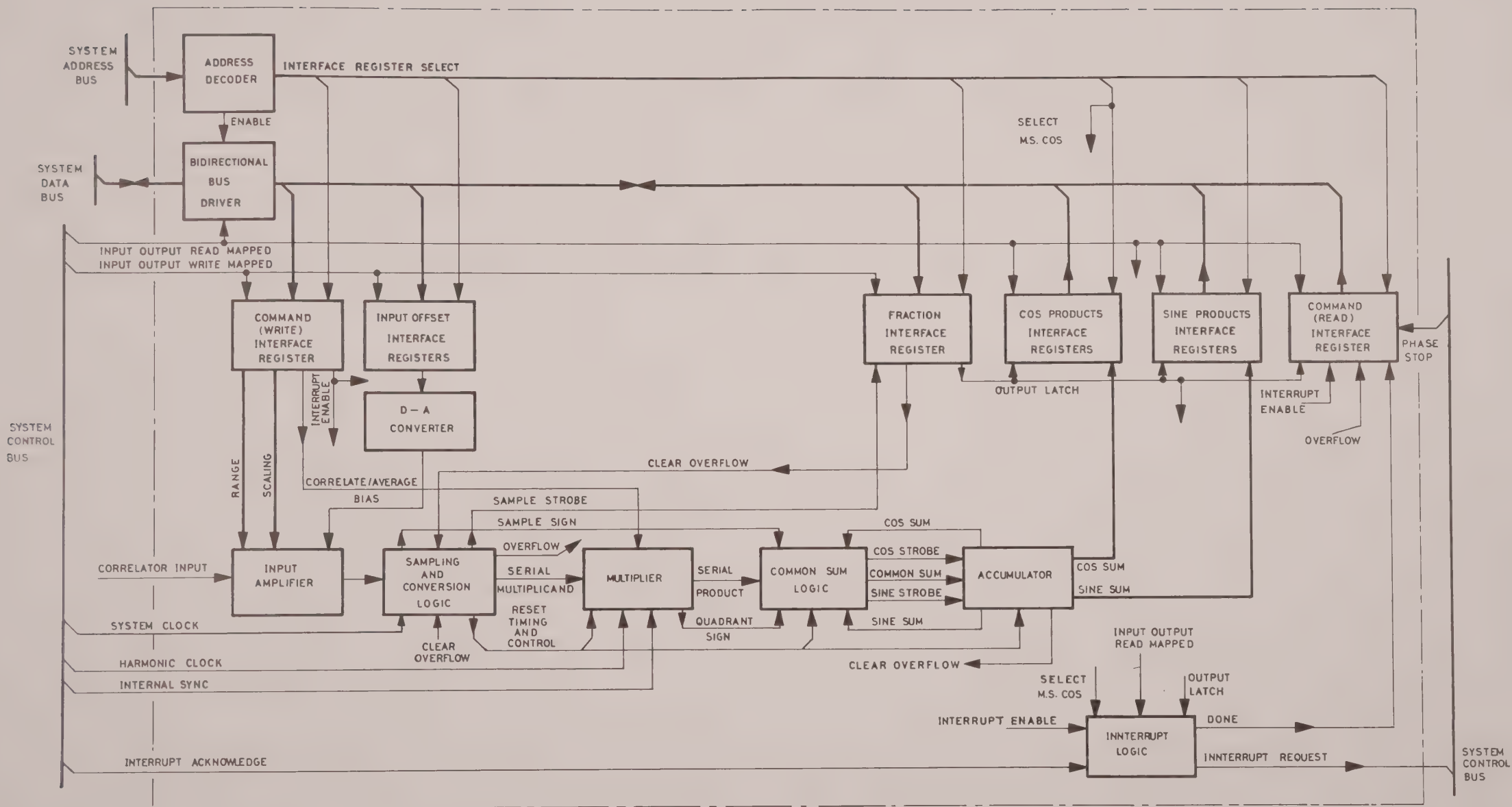
Correlator Status

The current states of INTERRUPT ENABLE, OVERFLOW and DONE, together with that of the PHASE STOP input from the Generator, are loaded into the Command (Read) Interface Register at the end of each set of samples. The contents of the Register thus give an indication of the correlator status at that time.

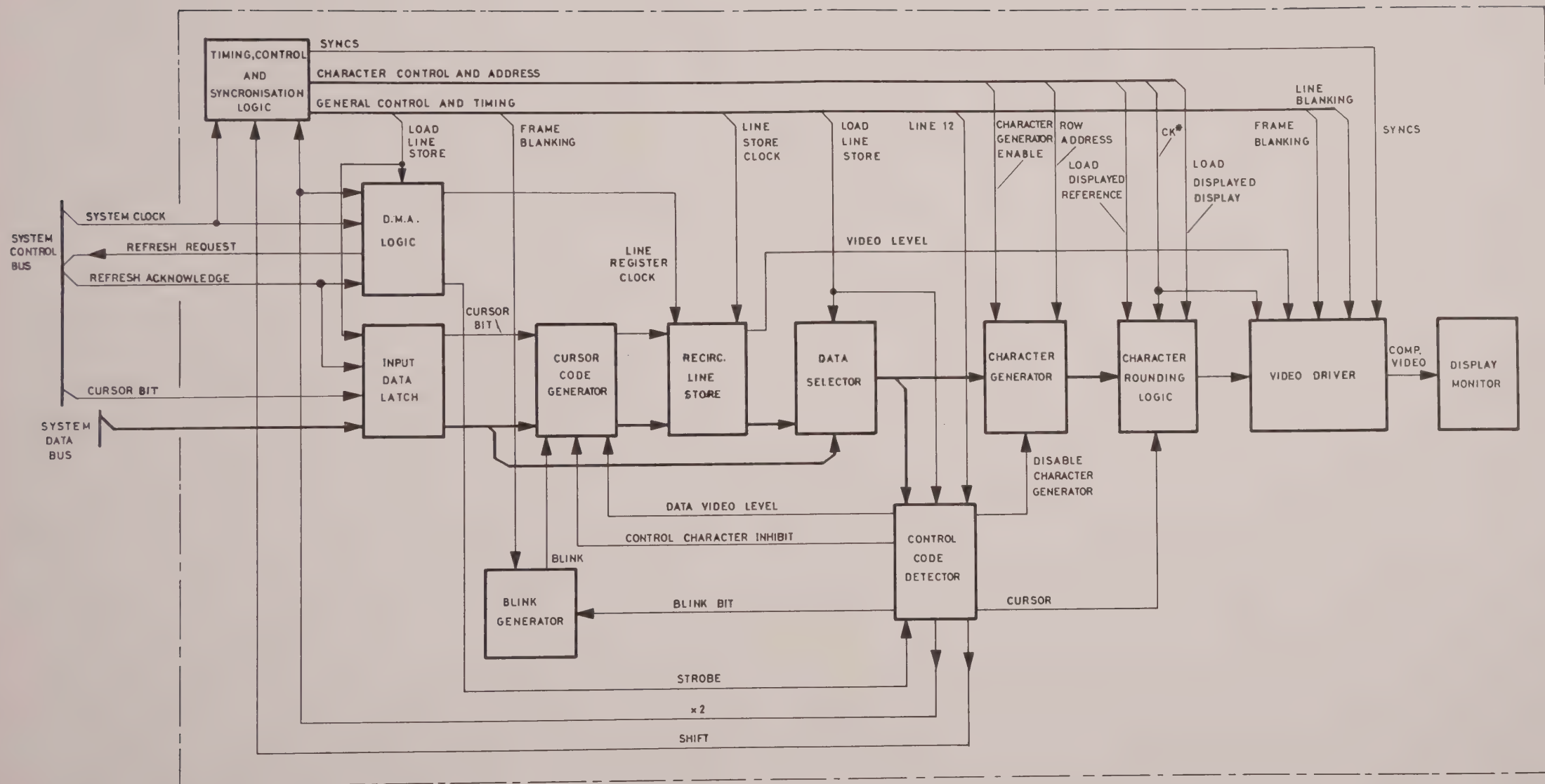
DISPLAY

The Display function (fig. 5.2.5) contains all the circuits and facilities necessary to enable any data input to the function via the System Data Bus to be presented to the Operator in the form of a visual (c.r.t.), alphanumeric display.

The c.r.t. display accommodates up to 512 characters in a 32-column x 16-row matrix (see section 4). Within this matrix, each character is allocated a 10-dot x 16-t.v. line character cell. Normally, only the first nine t.v. lines of the cell are used for the character; however, for lower-case characters with hangers (e.g. p), the first three lines



CORRELATOR FIG 5.2.4.



DISPLAY FIG 5.2.5.

are not used but the next nine are. Certain categories of data are displayed in double-size characters; in such cases, the character cell height is increased to 32 t.v. lines and character rounding is applied to improve legibility. The selection of data for double-size display is controlled by program.

The function circuits can be divided into three main areas:

- (a) The timing, control and synchronisation circuits, which generate the signals required for the basic timing and control of the generation of the video pattern that is to be displayed and to synchronise the c.r.t. display of the pattern.
- (b) The video pattern generator, which provides the video signal appropriate to the incoming character data and control codes.
- (c) The Display Monitor, which provides the means of displaying the video signal.

Timing, Control and Synchronisation

In the Timing, Control and Synchronisation Logic, the 6.144 MHz SYSTEM CLOCK is divided down to obtain a range of timing signals which provide the main timing references for the display operations. Milestone events marked by signals within this range are as follows:

- (a) Character period - A $1.63\ \mu\text{s}$ period signal indicates the boundaries of each display matrix column within each t.v. line.
- (b) T.V. line - The t.v. line time is defined as $63.48\ \mu\text{s}$. This is equivalent to thirty-nine display matrix columns. However, as seven of these columns occur during the line blanking period, the displayed matrix contains only thirty-two columns.
- (c) Data line - A $1.02\ \text{ms}$ period signal indicates the boundaries of each data line (i.e. each group of 16 t.v. lines).
- (d) Frame blanking - The t.v. frame blanking pulse is generated as a $2.03\ \text{ms}$ duration pulse at a period of $18.28\ \text{ms}$. The t.v. frame time is thus equivalent to that required to complete eighteen data lines. However, as the last two data lines occur during the frame blanking period, the displayed matrix contains only sixteen rows.

The Logic then suitably decodes these main timing signals to provide the three groups of timing, control and synchronisation signals indicated in fig. 5.2.5.

Generation of Video Pattern (Single-Size Mode)

Loading Display Data. At the end of the twelfth t.v. line of each data line, the Timing, Control and Synchronisation Logic makes the LOAD LINE STORE signal true for the remainder of the data line period. This causes the D.M.A. Logic to issue a REFRESH REQUEST to the Microprocessor via the System Control Bus, initiating a direct memory access (D.M.A.) which results in the 7-bit ASCII code for the first character position in the next data line appearing on the System Data Bus, and which enables the Input Data Latch.

The Microprocessor indicates that it is honouring the request by generating REFRESH ACKNOWLEDGE for some 200 ns. The arrival of this acknowledgement causes the D.M.A. Logic to terminate the request, while the trailing edge of the signal loads the contents of the System Data Bus - and the CURSOR BIT indication from the System Control Bus - into the Input Data Latch. The removal of REFRESH ACKNOWLEDGE also enables the D.M.A. Logic to raise another REFRESH REQUEST, resulting in the code and cursor information appropriate to the second character position entering the Display function.

The sequence described in the preceding paragraph repeats until the information for all thirty-two character positions in the data line has been obtained, at which time the D.M.A. Logic ceases to generate requests regardless of the state of the LINE STORE LOAD signal.

Shortly after the trailing edge of REFRESH ACKNOWLEDGE, the D.M.A. Logic generates a pair of LINE REGISTER CLOCK pulses. Thus providing it does not constitute a control code (see below), the data at the output of the Input Data Latch is loaded twice into the Recirculating Line Store via the Cursor Code Generator. Hence by the end of t.v. line 16 of the current data line, all the ASCII codes for the characters which are to be displayed in the next data line are in the Line Store, in the correct sequence and with each complete code appearing at each of a pair of consecutive store locations.

Generation of Video Character Data. During t.v. lines 1 to 12 of each data line, the Timing, Control and Synchronisation Logic generates a LINE STORE CLOCK pulse train which is at twice the rate of the character period and synchronised such that a pulse appears at the beginning of, and midway through, each character period. This clock is used to circulate the data within the Line Store. In the absence of LOAD LINE STORE, the Data Selector selects the Line Store output to the Character Generator and the Control Code Detector. Thus twice per character period, the ASCII code appropriate to the character which is to be displayed during that period is input to the Generator and the Detector.

The Character Generator is a read-only memory (ROM) which contains all the information required to enable the generation of the video signals appropriate to the unrounded form of each of the various characters. A group of sequential addresses is allocated to each character, each address corresponding to a particular t.v. line in the character cell and each bit of the parallel word in that address corresponding to a particular dot position on that line.

With normal characters, the Generator is enabled from the beginning of t.v. line 1 to the end of t.v. line 9; for lower-case characters with hangers, it is enabled from the beginning of t.v. line 4 to the end of t.v. line 12. The Generator address is obtained from two sources, the 7-bit character code being used as the m.s. portion, while the l.s. portion is provided by the 4-bit ROW ADDRESS code. The latter changes for each t.v. line during the data line. Thus the character code locates the block of addresses containing the character information, while the ROW ADDRESS accesses the address within the block corresponding to the t.v. line currently in progress.

As the end of the character period approaches, a LOAD DISPLAYED REFERENCE pulse loads the character information currently being output

from the Character Generator into the Character Rounding Logic. In the single-size mode, the latter is ineffective and so the information passes through the Logic without modification and serially to the Video Driver under the control of clock CK*.

Video Output. At the input of the Video Driver, the character information is OR'ed with the FRAME BLANKING and LINE BLANKING signals. The amplitude of the result of this operation is then adjusted in accordance with the state of the VIDEO LEVEL indicator before it is mixed with the SYNC signal to form the COMPOSITE VIDEO signal required by the Display Monitor.

Control Code Processing. During the period of LOAD LINE STORE, the Data Selector routes the 7-bit ASCII code output of the Input Data Latch directly to the input of the Control Code Detector, where it is examined for video attribute and double-size character control codes. If such a code is detected, then the STROBE signal which the D.M.A. Logic generates in response to each REFRESH ACKNOWLEDGE causes the Control Code Detector to output CONTROL CHARACTER INHIBIT to the Cursor Code Generator, resulting in a Null character being loaded into the Recirculating Line Store.

Four video attribute control codes are provided. Under the control of program, these are used as required to attribute one of the following combinations of video characteristics to each field of data presented to the Operator:

- (a) Steady, bright display.
- (b) Flashing, bright display.
- (c) Steady, dim display.
- (d) Flashing, dim display.

The Control Code Detector signals the requirement for a bright or a dim display by clearing, or setting, respectively, the DATA VIDEO LEVEL signal applied to the m.s. input of the Cursor Code Generator. Thus when the next character (i.e. the first character which is to exhibit the attribute) is loaded into the Recirculating Line Store, it is accompanied by a VIDEO LEVEL bit of the correct state. Each time the character is applied to the Character Generator, therefore, the VIDEO LEVEL bit is applied to the Video Output stage to adjust the amplitude of the data component of the COMPOSITE VIDEO such as to obtain the required display intensity.

When a flashing field is required, the first character of that field is preceded by a 'flashing' control code, causing the Control Code Detector to output BLINK BIT to the Blink Generator. At the latter, BLINK BIT is gated with a signal which is FRAME BLANKING divided by 32, and so the BLINK input to the Cursor Code Generator is a signal which is active for the period of each thirty-second frame. Like CONTROL CHARACTER INHIBIT, the presence of BLINK causes a Null character to be loaded into the Line Store. Thus during every thirty-second frame, the selected field or fields will not be written to the display, causing those fields to appear to flash.

If the double-size character control mode is detected, the Detector generates a x2 output. This is passed to the Timing, Control and Synchronisation Logic and D.M.A. Logic, with the results described later.

Abnormal Character and Cursor Code Processing. During t.v. lines 1 to 12, the Data Selector passes to the Control Code Detector the character codes being read out of the Recirculating Line Store for display. The Detector then examines the codes for those demanding lower-case characters with hangers, Null characters or Cursor characters.

When a lower-case character with a hanger is detected, SHIFT is sent to the Timing, Control and Synchronisation Logic, where it causes the ROW ADDRESS for the Character Generator to be modified so as to allow character data to be displayed on the three t.v. lines below the normal character base line.

When a Null character code or Cursor code is detected, the Character Generator is disabled, causing 'all ones' to be loaded into the Character Rounding Logic. With a Null character, no further action is taken during the character period and so no character is written to the display. However, if it is a Cursor Code, then at the beginning of t.v. line 12, LINE 12 from the Timing, Control and Synchronisation Logic causes the Detector to generate CURSOR, which clears the Character Rounding Logic registers. Thus the cursor appears as a seven-dot bar on t.v. line 12.

Generation of Video Pattern (Double-Size Mode)

While the operation of the video pattern generator circuits in this mode is generally similar to that described for the previous mode, there are a number of important differences, as described below.

Loading Display Data. In the double-size mode, each incoming code and accompanying VIDEO LEVEL must be loaded into four consecutive locations in the Recirculating Line Store. The x2 input to the D.M.A. Logic enables this by causing that logic to produce four LINE REGISTER CLOCK pulses, per refresh; also, it causes the next REFRESH REQUEST to be delayed sufficiently to allow this loading to take place.

Row Addressing. The x2 input to the Timing, Control and Synchronisation Logic modifies the ROW ADDRESS sequence so that during each t.v. line of the character, two addresses (Reference and Display) are generated to extract the data required to enable character rounding to be applied.

Character Rounding. During x2 operation, the rate of the control signals to the Character Rounding Logic is halved and, as indicated above, both reference and display codes are made available to the Logic. This allows the logic to become effective so that the rounded form of the character is displayed.

Display Monitor

The Display Monitor is a conventional, general-purpose data display requiring only the connection of the appropriate power supply lines and input signal to enable its operation.

KEYBOARD

The function of the Keyboard (fig. 5.2.6) is to provide the F.R.A. with a man-machine interface via which the Operator can enter commands and data (see section 4).

The 40-station Keyswitch Matrix is repetitively interrogated on a station-by-station basis. If, during the interrogation period allocated to a particular keyswitch, the matrix output indicates that the keyswitch is in - or has assumed - the operated condition, the Keyswitch Scanner and Detector outputs to the ASCII Encoder a 6-bit code specific to that keyswitch. The Encoder responds to the keyswitch code by passing to the associated input of the Programmable Interface the 7-bit ASCII code appropriate to the keyswitch character or function. Shortly afterwards, the Keyswitch Scanner and Detector strobes the ASCII code into the interface device. If interrupts are allowed, the trailing edge of the STROBE pulse causes the Programmable Interface to generate an INTERRUPT REQUEST.

The Keyboard interfaces with the System Data Bus via three registers contained in the Programmable Interface:

- (a) The Keyboard Data Register, a read only register used to hold the ASCII code.
- (b) The Keyboard Status Register, a read only register used to indicate the current status of the Keyboard (e.g. whether or not the Data Register contains valid data).
- (c) The Keyboard Control Register, a write only register used to hold the control data which defines the mode of operation of the Programmable Interface and whether or not interrupts are allowed.

As elsewhere in the system, these registers are accessed by placing the required vector and port addresses on the System Address Bus and applying an INPUT OUTPUT READ or INPUT OUTPUT WRITE pulse as appropriate.

POWER SUPPLY

The Power Supply Assembly provides all the d.c. supplies necessary for the operation of the F.R.A. other than these used within the Display Monitor circuits. The assembly outputs are divided into four groups:

- (a) Group 1 (earthy supplies) - Microprocessor, Memory, Display, Keyboard, Options;

- + 5V 10A (15A fuse)
 - +12V 2.5A (4A fuse)
 - 12V 2A

- (b) Group 2 (floating supplies) - Generator; Ext. Sync. Bd;

- + 5V 0.5A
 - +30V 0.5A
 - 30V 0.5A

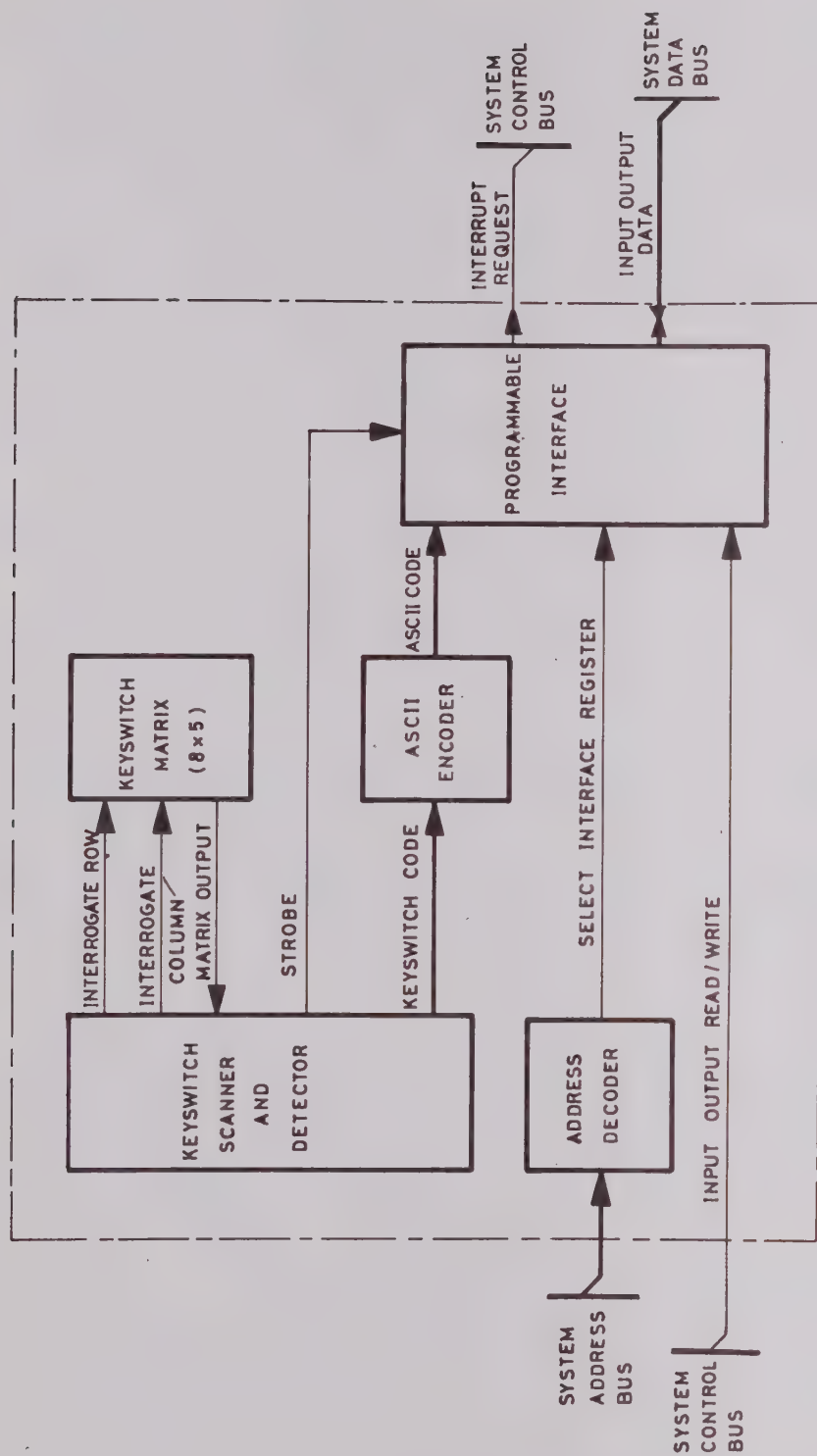


FIG 5.2.6. KEYBOARD

(c) Group 3 (floating supplies) - Correlator 1,Ext.Sync.Generator:

+ 5V	0.5A
+30V	0.5A
-30V	0.5A

(d) Group 4 (floating supplies) - Correlator 2;

+ 5V	0.5A
+30V	0.5A
-30V	0.5A

ALPHANUMERIC DISPLAY

Introduction

The alphanumerics control board contains most of the facilities originally contained on the two display control boards, and is a replacement for both boards. It is fitted into socket SKT7 on the motherboard. The double-height character facility has been deleted and the board re-designed to allow the graphics control board option to be used in conjunction with this board. Operation of the SE 2450 is unaffected by fitting the alphanumerics control board option. Only the appearance of the display is affected.

Display Features

The display generated by this board accommodates up to 512 characters in a 32-column x 16 row matrix. Within this matrix, each character is allocated a 10 dot x 16 TV line character cell. Normally only the first 12 lines of the cell are used for display, the other four lines remaining blank. The full 128 ASCII character set is contained in a ROM on the board, including upper and lower case characters and control characters.

A cursor can be displayed together with any character in any position, the display alternating between character and cursor once per second. A group of consecutive characters can be made to flash on and off or can be displayed bright or dim.

Theory of Operation (Fig 5.2.9)

A data string of 32 characters in 7-bit ASCII code, together with a cursor bit, is transferred from the main memory, via the system data bus to a re-circulating store on the alphanumeric control board. This data, sufficient for one row of displayed characters, is obtained using direct memory access (DMA) under the control of the DMA logic on the board.

The data is then cycled through the recirculating store 12 times, each time round representing one TV line of the display. As each data byte in turn is presented to the character generator ROM, the bit pattern for that TV line of the character is output from the ROM, converted to serial form by the video shift register, and output to the screen via the video driver.

During the following 4 blank TV line periods the recirculating store is cleared and the next 32 characters are loaded in from the main memory. This process is repeated 16 times per TV frame to complete the display.

The control code detector receives the data at the same time as the character generator, and produces control signals to operate the flashing and bright/dim facilities, and to inhibit display of control codes.

The timing control and synchronisation circuits generate all the signals required for the generation of the alphanumeric video pattern and for the control of all the other facilities on the board.

Timing, Control and Synchronisation

In the timing, control and synchronisation logic, the 6.133 MHz SYSTEM CLOCK is divided down to obtain a range of timing signals which provide the main timing references for the display operations. Milestone events marked by signals within this range are as follows:

- (a) **Character Period D:** A $1.63\mu\text{s}$ period signal indicates the boundaries of each display matrix column within each TV line.
- (b) **TV Line.** The TV line time is $63.48\mu\text{s}$, which is equivalent to thirty-nine display matrix columns. However, as seven of these columns occur during the line blanking period, the displayed matrix contains only thirty-two columns.
- (c) **Data Line.** A 1.02 ms period signals indicates the boundaries of each line (i.e. each group of 16 TV lines)
- (d) **Frame Blanking.** The TV frame blanking pulse is generated as a 2.03 ms duration pulse at a period of 18.28 ms. The TV frame time is thus equivalent to that required to complete eighteen data lines. However, as the last two data lines occur during the frame blanking period, the displayed matrix contains only sixteen rows.

The logic then suitably decodes these main timing signals to provide the three groups of timing, control and synchronisation signals indicated in fig 5.2.9.

Generation of Video Pattern

Loading Display Data. At the end of the twelfth TV line of each data line, the timing, control and synchronisation logic activates the LOAD LINE STORE (LLS) signal for the remainder of the data line period. This causes the DMA logic to issue a REFRESH REQUEST (RFRQ) to the microprocessor via the system control bus, initiating a direct memory access (DMA) which places the 7-bit ASCII code for the first character position in the next data line, on the system data bus, and enables the input data latch.

The microprocessor indicates that it is acknowledging the request by generating REFRESH ACKNOWLEDGE for some 200 ns. The arrival of this acknowledgement causes the DMA logic to terminate the request, while the trailing edge of the signal loads the contents of the system data bus - and the CURSOR BIT indication from the system control bus - into the input data latch. The removal of REFRESH ACKNOWLEDGE also enables the DMA logic to issue another REFRESH REQUEST, resulting in the code and cursor information appropriate to the second character position entering the input data latch.

The sequence described in the preceding paragraph repeats until the information for all thirty-two character positions in the data line has been obtained, at which time the DMA logic ceases to generate requests regardless of the state of the LINE STORE LOAD signal.

Generation of Video Character Data. During TV lines 1 to 12 of each data line, the timing, control and synchronisation logic generates LINE STORE INPUT and OUTPUT clock pulses, which are used to circulate the data within the line store. In the absence of LOAD LINE STORE, the output data selector directs the line store output to the character generator and the control code detector. Thus once per character period, the ASCII code appropriate to the character which is to be displayed during that period is input to the generator and the detector.

The character generator is a read-only memory (ROM) which contains all the information required to enable the generation of the video signals appropriate to each of the various characters. A group of sequential addresses is allocated to each character, each address corresponding to a particular TV line in the character cell and each bit of the parallel word in that address corresponding to a particular dot position on that line.

The generator address is obtained from two sources, the 7-bit character code being used as the m.s. portion, while the l.s. portion is provided by the 4-bit ROW ADDRESS code. The latter changes for each TV line during the data line. Thus the character code locates the block of addresses containing the character information, while the ROW ADDRESS accesses the address within the block corresponding to the TV line currently in progress.

The output of the ROM is loaded into the video shift register by the D waveform, and is then shifted out serially by the Ø3 clock, which runs at ten times the rate of D, giving 10 dots across the character cell. Seven dots represent character information, the other 3 being blanks.

Video Output. At the input of the video driver, the character information is OR'ed with the FRAME BLANKING and LINE BLANKING signals. The amplitude of the result of this operation is then adjusted in accordance with the state of the VIDEO LEVEL indicator before it is mixed with the SYNC signal to form the COMPOSITE VIDEO signal required by the display monitor.

Control Code Processing. During the period of LOAD LINE STORE, the data selector routes the 7-bit ASCII code output of the input data latch directly to the input of the control code detector, where it is examined for video attribute and control codes. If such a code is detected, then the STROBE signal which the DMA logic generates in response to each REFRESH ACKNOWLEDGE causes the control code detector to output CONTROL CHARACTER INHIBIT to the cursor code generator, resulting in a null character being loaded into the recirculating line store.

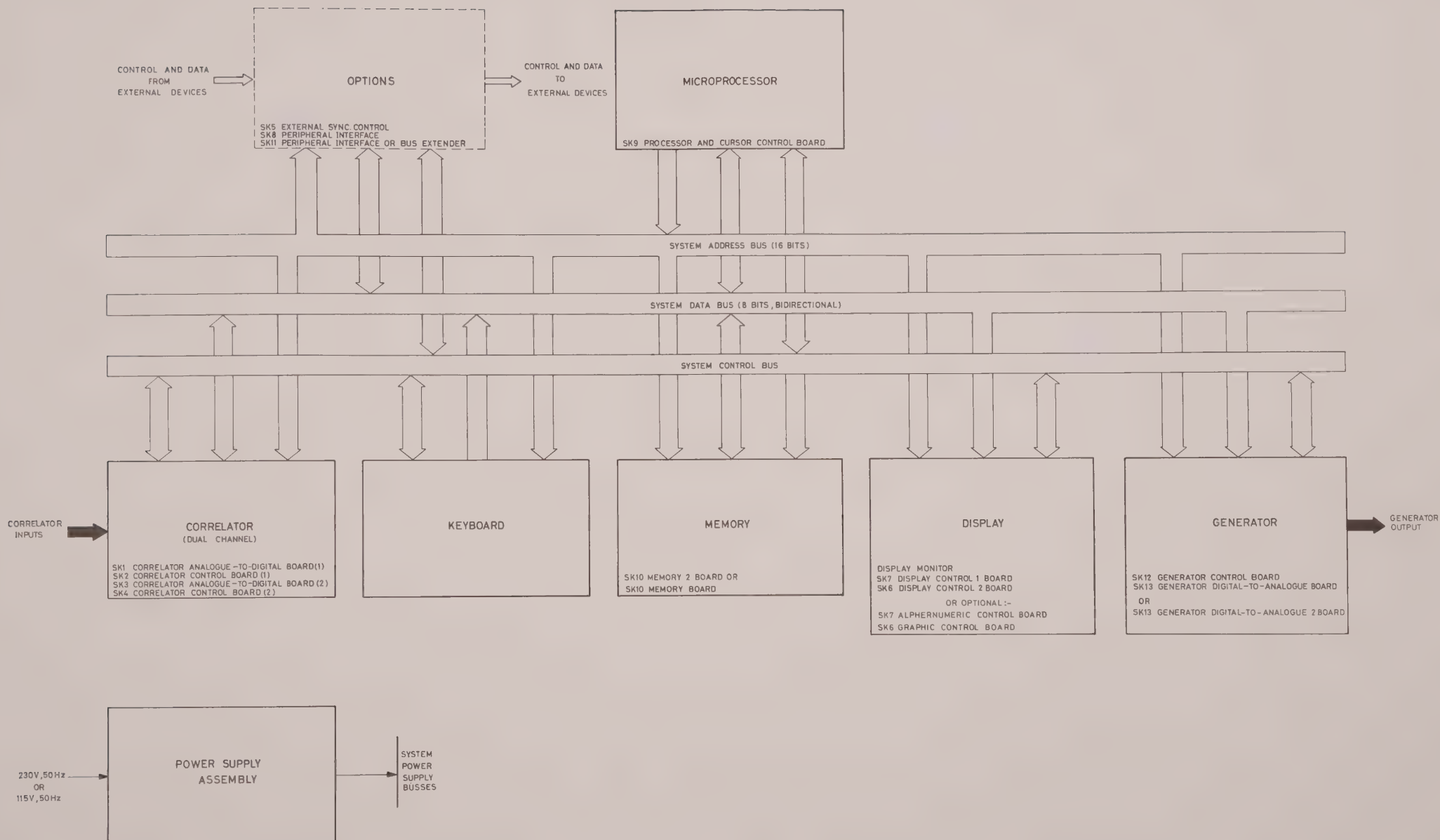
Four video attribute control codes are provided. Under the control of program, these are used as required to attribute one of the following combinations of video characteristics to each field of data presented to the operator; steady bright display, flashing bright display, steady, dim display, flashing dim display.

The control code detector signals the requirement for a bright or a dim display by clearing, or setting respectively, the DATA VIDEO LEVEL signal applied to the m.s. character data input of the cursor code generator. Thus when the next character (i.e. the first character which is to exhibit the attribute) is loaded into the recirculating line store, it is accompanied by a VIDEO LEVEL bit of the correct state. Each time the character is applied to the character generator, therefore, the VIDEO LEVEL bit is applied to the video output stage to adjust the amplitude of the data component of the COMPOSITE VIDEO such as to obtain the required display intensity.

When a flashing field is required, the first character of that field is preceded by a flashing control code, causing the control code detector to output BLANK BIT to the blink generator. At the latter, BLINK BIT is gated with a signal which is FRAME BLANKING divided by 32, and so the BLINK input to the cursor code generator is a signal which is active for the period of 32 frames. Like CONTROL CHARACTER INHIBIT, the presence of BLINK causes a null character to be loaded into the line store, instead of the selected fields, causing those fields to appear to flash.

Cursor Code Processing

When a cursor bit is received it is ANDed with the blink bit BL1 and the result is used to switch on the cursor code generator, and a 7-bit cursor code is fed into the recirculating store instead of the character data for that position. The cursor code is output to the character generator ROM at the correct times and the cursor video data is output to the video shift register. The blink bit causes the cursor code generator to switch between cursor code and normal character code at the blink rate displaying cursor and character alternately.



F.R.A. SYSTEM FIG 5.2.7

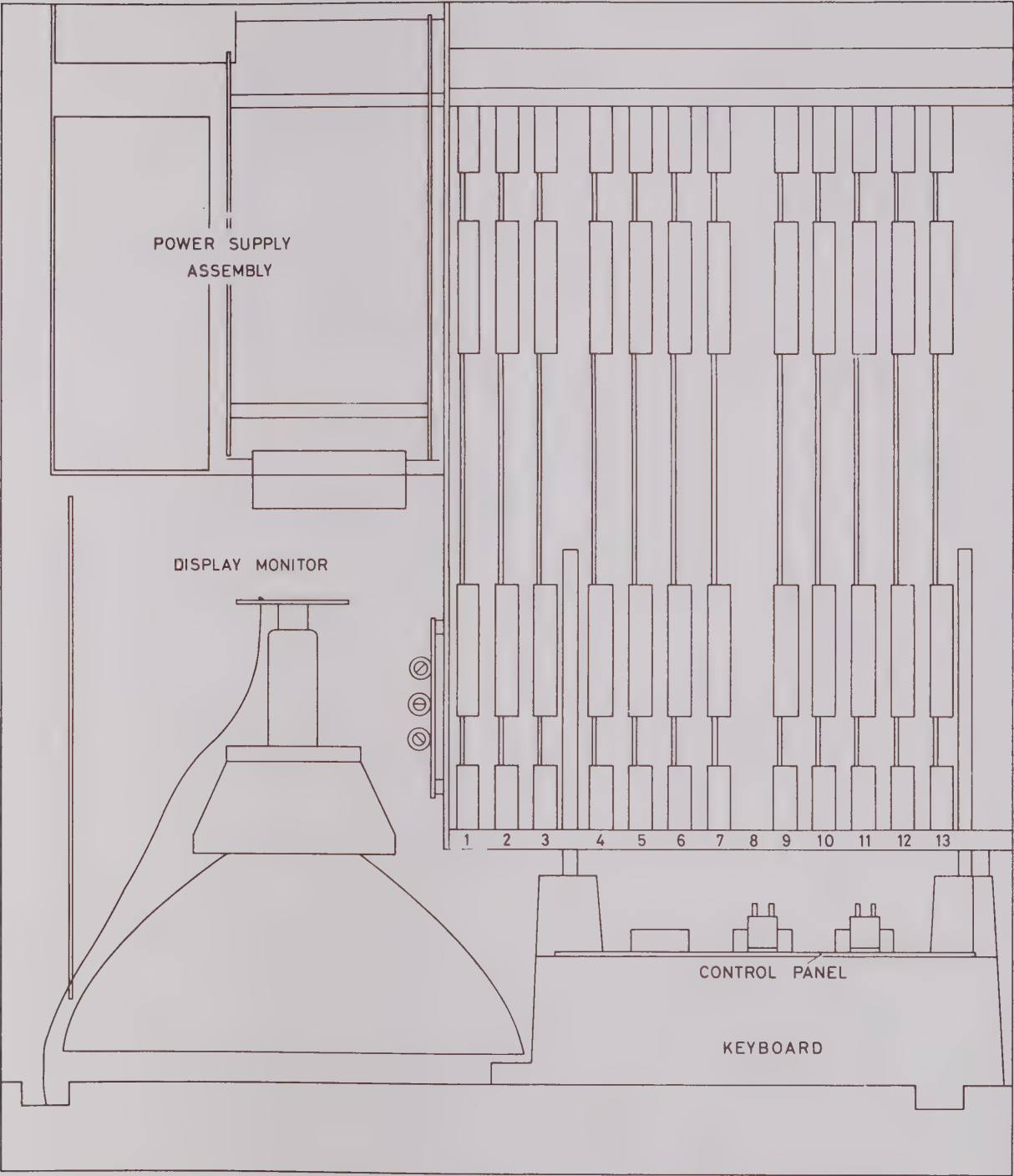
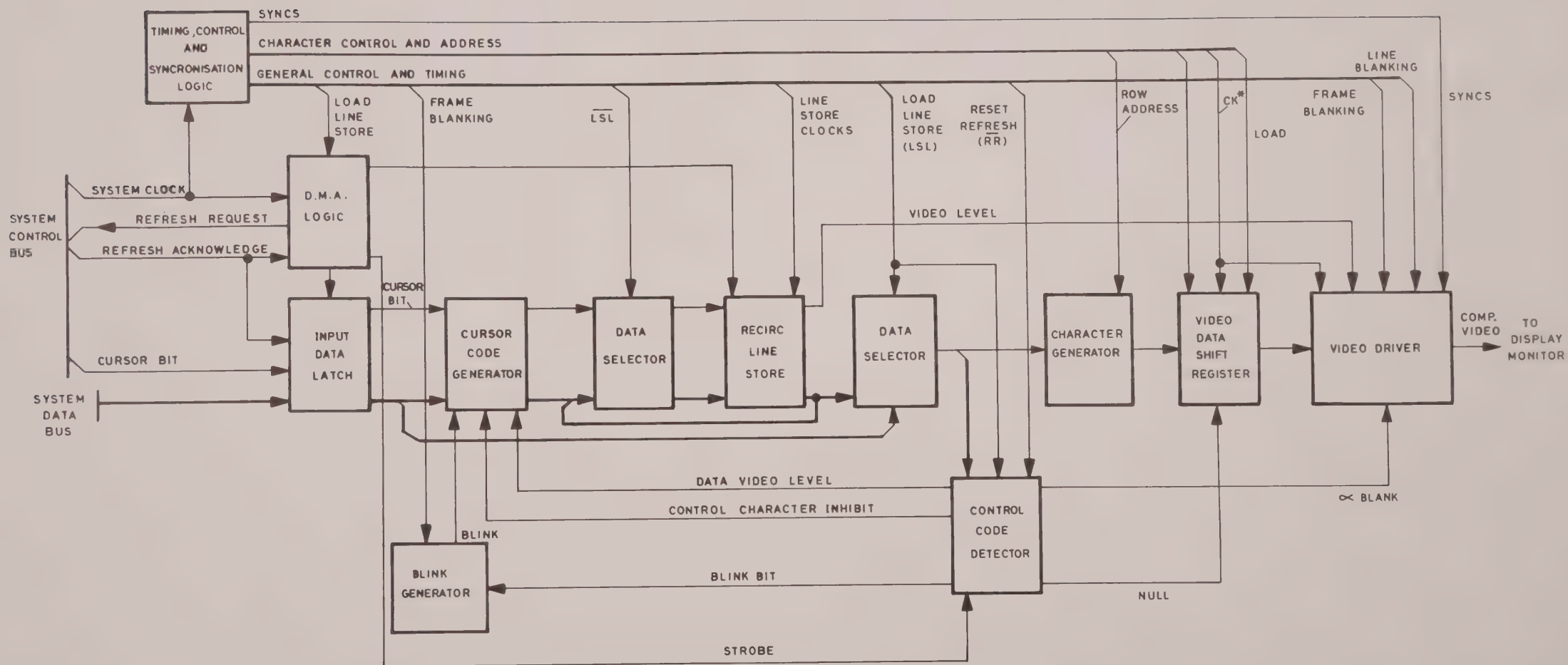


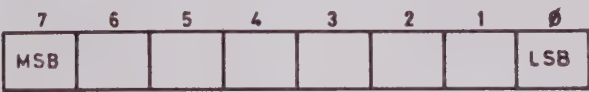
FIG 5.2.8 F.R.A. LAYOUT



ALPHANUMERIC DISPLAY SYSTEM FIG.5.2.9.

INTRODUCTION

The bit assignments of the Frequency Response Analyser peripheral interface registers are assigned as are the vector and port address of the peripheral devices. In the context of this chapter all addresses are hexadecimal radix, unless otherwise stated, and the mnemonics specified for the bits are for hardware use only. The mnemonics specified for the registers are used for both hardware and software. All mnemonics are shown in parenthesis unless otherwise stated. Bit assignment diagrams for the various registers comply with the following convention:



where, 7-0 are the bit numbers and MSB and LSB are the most significant and least significant bits respectively.

PORT ADDRESS ALLOCATIONS

The port address allocations for the FRA peripheral registers are given in Table 5.3.1. In this table the letters 'R', 'W' and 'R/W' indicate the type of register, i.e. read, write and read/write respectively.

ASSIGNMENTS OF RESTART VECTORS

The assignments of the restart vectors for the FRA peripheral registers are the same as that of the peripheral devices, and are as per the following table.

TABLE 5.3.2 ASSIGNMENTS OF RESTART VECTORS

INTERRUPT	VECTOR	DEVICE 1	DEVICE 2
7	0	Power-Up	-
6	1	Correlator 1	Correlator 2
5	2	External Sync	-
4	3	Serial I/F.(CCITT V24)	Parallel I/F.(IEEE 488)
3	4	X-Y Plotter	-
2	5	Generator	-
1	6	Integral Keyboard	-
0	7	Diagnostics	-

TABLE 5.3.1 : PORT ADDRESS ALLOCATION TABLE

	PORT ADDRESS	MNEMONIC	TYPE	CONTENTS
IEEE 488 INTERFACE REGISTERS	30	DAT IN	R	Data In
		DAT OUT	W	Data Out
	31	INTS1	R	Interrupt Status 1
		INTM1	W	Interrupt Mask 1
	32	INTS2	R	Interrupt Status 2
		INTM2	W	Interrupt Mask 2
	33	SPS	R	Serial Poll Status Register
		SPM	W	Serial Poll Mode Register
	34	ADDRS	R	Address Status Register
		ADDRM	W	Address Mode Register
	35	CPT	R	Command Pass Through Register
		AUXMOD	W	Auxiliary Mode Register
	36	ADDR0	R	Address 0 Register
		ADDR0/1	W	Address 0/1 Register
	37	ADDR1	R	Address 1 Register
		EOS	W	End of Sequence Register
	38	BADDR	R	Bus Address Register
GENERATOR REGISTERS	40	GAM	W	Generator Amplitude MS byte
	41	GAL	W	Generator Amplitude LS byte
	42	GFM	W	Generator Frequency Mantissa MS byte
	43	GFL	W	Generator Frequency Mantissa LS byte
	44	GER	W	Generator Frequency Exponent
	45	GHR	W	Generator Harmonic Register
	46	GEP	W	Generator End Phase
	47	GBR	W	Generator Bias Register

TABLE 5.3.1 PORT ADDRESS ALLOCATION TABLE (cont)

	PORT ADDRESS	MNEMONIC	TYPE	CONTENTS
CORRELATOR 1 REGISTER	48	CCR1	R/W	Correlator 1 Command Register
	49	OFF M1	W	Correlator 1 Input Offset MB byte
	4A	OFF L1	W	Correlator 1 Input Offset LS byte
	4B	CRF1	W	Correlator 1 Fraction Register
	4C	CSD M1	R	Correlator 1 Sine Product MS byte
	4D	CSD L1	R	Correlator 1 Sine Product LS byte
	4E	CCD M1	R	Correlator 1 Cosine Product MS byte
	4F	CCD L1	R	Correlator 1 Cosine Product LS byte
EXTERNAL SYNC REGISTERS	50	XSYN	R/W	External Sync Command/Status Register
	51	-	R/W	Reserved
	52	-	R/W	Reserved
	53	-	R/W	Reserved
	54	XSYNC1	R	External Period Measurement MS byte
	55	XSYNC2	R	External Period Measurement LS byte
	56	XSYNC3	R	External Period Measurement 2nd.MS byte
	57	XSYNC4	R	External Period Measurement 2nd.LS byte
KEYBOARD REGISTERS	58	KB CTL	W	Keyboard Control Register
	59	KB STAT	R	Keyboard Status Register
	5A	-	-	Not Used
	5B	KB DAT	R	Keyboard Data (ASCII coding)
	5C	-	R/W	Reserved
	5D	-	R/W	Reserved
	5E	-	R/W	Reserved
	5F	-	R/W	Reserved

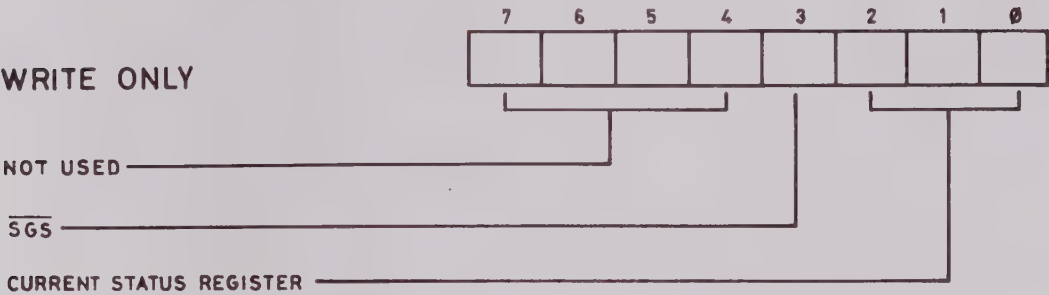
TABLE 5.3.1. PORT ADDRESS ALLOCATION TABLE (cont)

	PORT ADDRESS	MNEMONIC	TYPE	CONTENTS
CORRELATOR 2 REGISTERS	60	CCR2	R/W	Correlator 2 Command Register
	61	OFF M2	W	Correlator 2 Input Offset MS byte
	62	OFF L2	W	Correlator 2 Input Offset LS byte
	63	CFR2	W	Correlator 2 Fraction Register
	64	CSD M2	R	Correlator 2 Sine Product MS byte
	65	CSD L2	R	Correlator 2 Sine Product LS byte
	66	CCD M2	R	Correlator 2 Cosine Product MS byte
	67	CCD L2	R	Correlator 2 Cosine Product LS byte
CCITT V24 SERIAL INTERFACE 1	70	SIDAT1	R/W	Serial Interface 1 Data byte
	71	SICTS1	R/W	Serial Interface 1 Control Status
CCITT V24 SERIAL INTERFACE 2	72	SIDAT2	R/W	Serial Interface 2 Data byte
	73	SICTS2	R/W	Serial Interface 2 Control Status
MISCELLANEOUS	74	-	-	Register reserved for future peripheral
	75	-	-	Register reserved for future peripheral
	76	-	-	Register reserved for future peripheral
	77	-	-	Register reserved for future peripheral
PROCESSOR REGISTERS	78	INTP	W	Processor Interrupt Priority
	7A	CADDL	W	Cursor Address L.S.B.
	7C	CADDM	W	Cursor Address M.S.B.

PROCESSOR REGISTERS

This sub-section briefly describes and shows the bit assignments for the Processor Registers.

Processor Interrupt Priority Register (INTP):79H

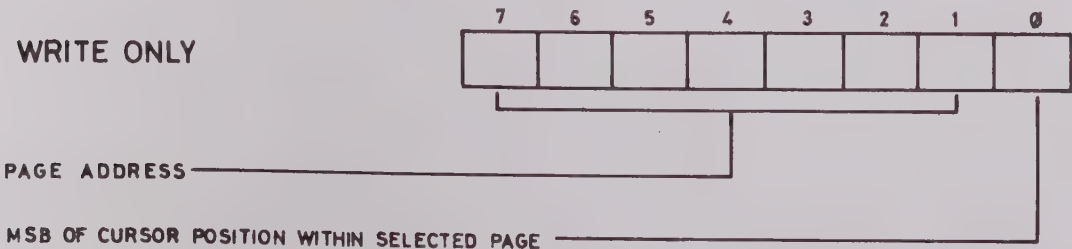


If SGS is high, service is given to the highest priority interrupt occurring (IRQ7). If SGS is low, an interrupt is only serviced if it is of a greater level than the complement of the number in the current status register. The bit assignments for the various interrupt priority levels for the register are as follows:

INTP								Lowest Interrupt Priority Allowed
7	6	5	4	3	2	1	0	
X	X	X	X	1	X	X	X	0
X	X	X	X	0	1	1	1	1
X	X	X	X	0	1	1	0	2
X	X	X	X	0	1	0	1	3
X	X	X	X	0	1	0	0	4
X	X	X	X	0	0	1	1	5
X	X	X	X	0	0	1	0	6
X	X	X	X	0	0	0	1	7
X	X	X	X	0	0	0	0	NONE

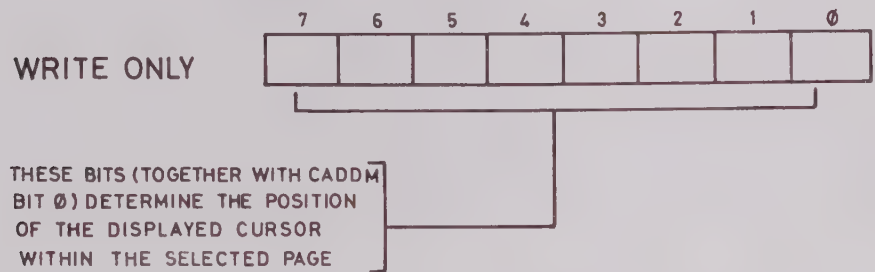
(X = don't care)

Cursor Address Register MSB (CADDM):7CH



The display consists of 16 lines of 32 characters each, thus giving 512 addressable cursor positions per page. The top-left-hand corner of the screen may reside at any 512 byte boundary within the RAM memory (i.e. 8000H to BFFFH). Bits 7-1 determine the page address, while bit 0 is the most significant bit of the actual cursor position within the select page. In effect, bit 0 selects which half of the page the cursor is positioned in.

Cursor Address Register LSB (CADDL):7AH

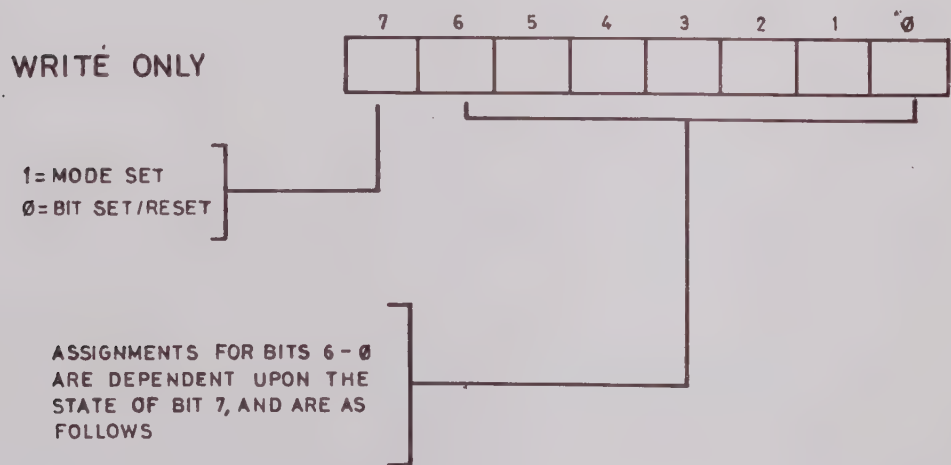


The cursor is only a visual aid as to where data may be written, in any position on any page.

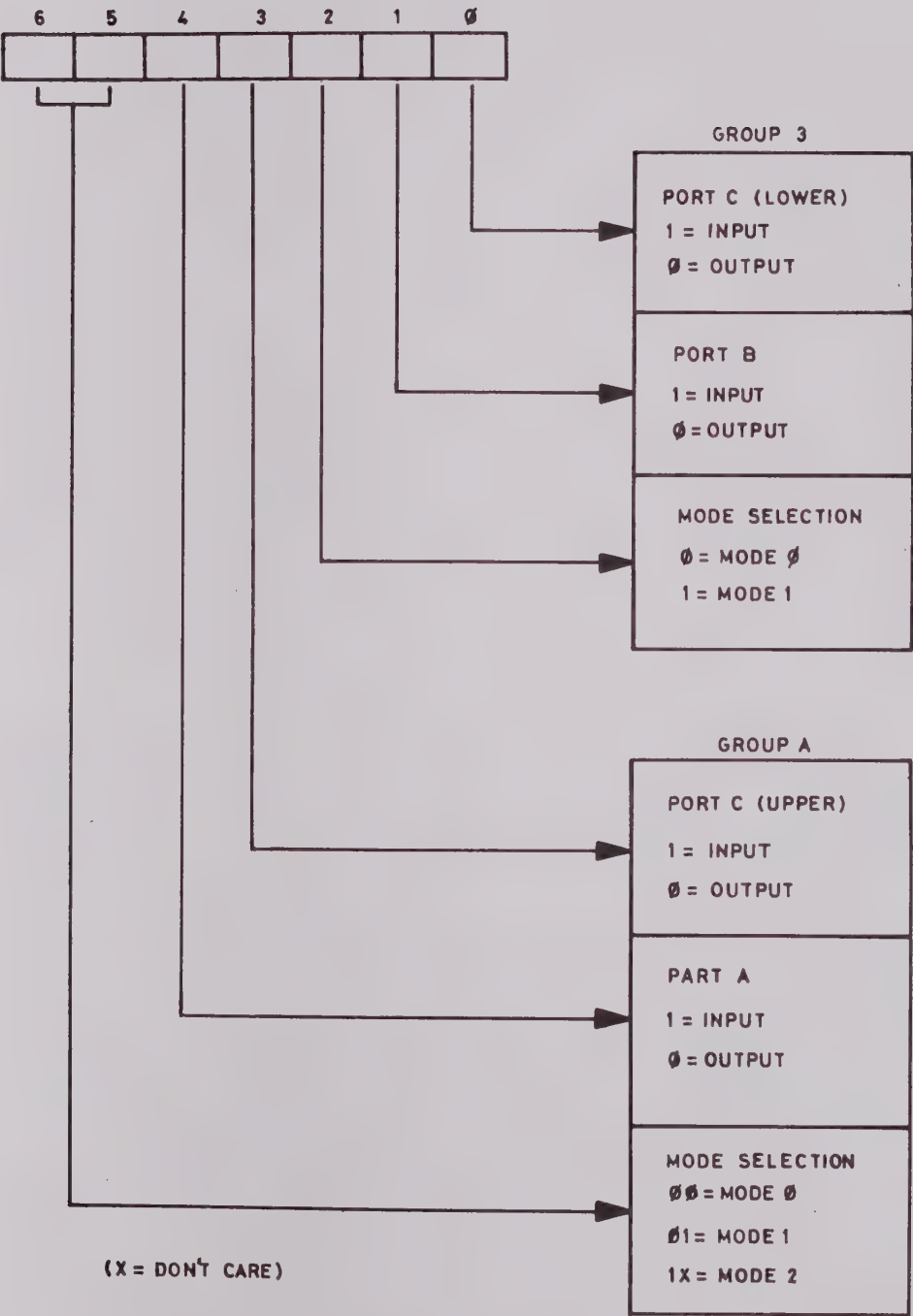
INTEGRAL KEYBOARD INTERFACE REGISTERS

This sub-section briefly describes and shows the bit assignments for the integral keyboard interface registers.

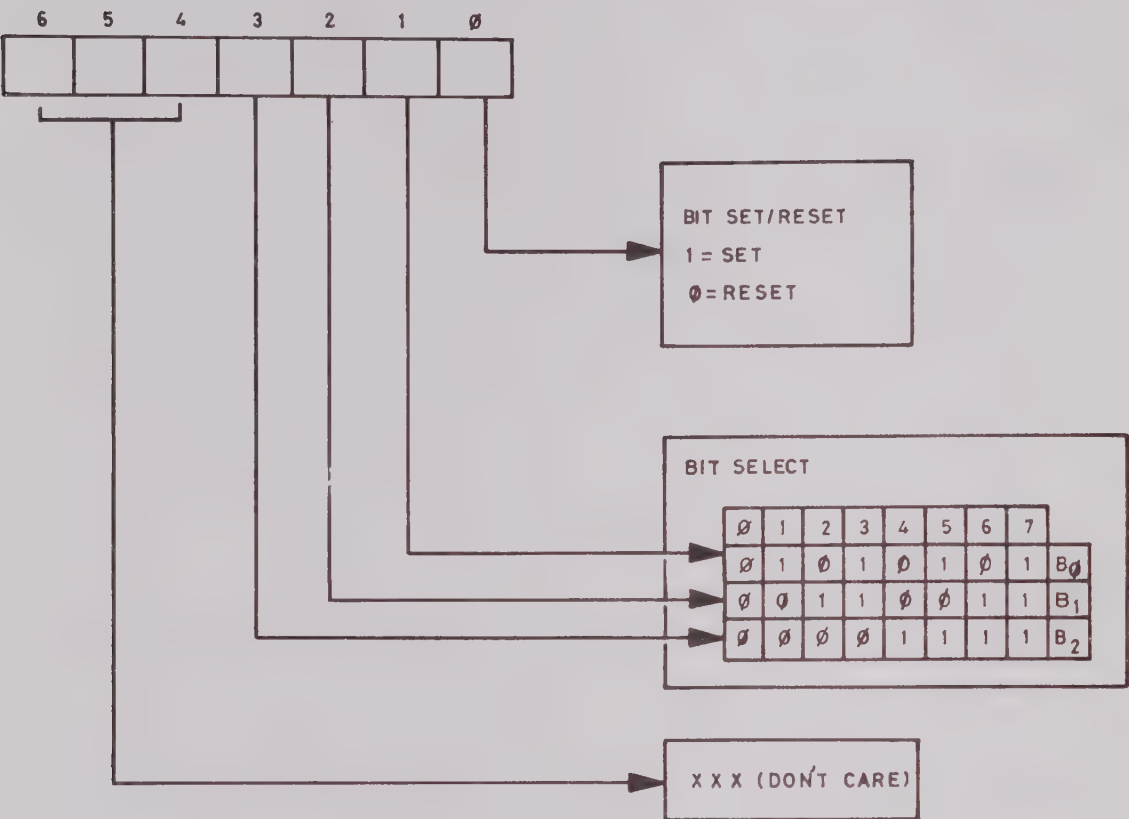
Keyboard Control Register (KBCTL):58H



If bit 7 is 1 (Mode Set) the assignment for bits 6-0 are as follows:



If bit 7 is 0 (Bit Set/Reset) the assignments for bits 6-0 are as follows:

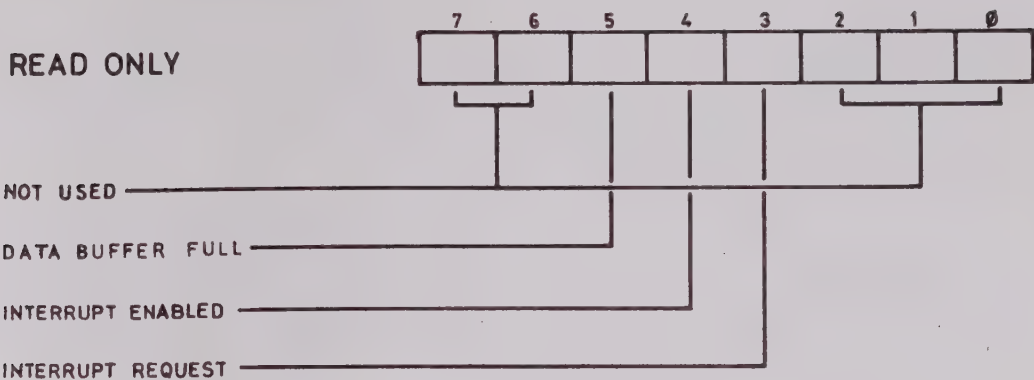


To initialise the keyboard after power-up, write B4H to the ports. Interrupts may be enabled or disabled using the bit set/reset function as follows:

Write 09H to KBCTL to enable interrupts, and write 08H to KBCTL to disable interrupts.

For further information regarding the operational characteristics etc., of this register, see Intel data sheet for Programmable Peripheral Interface device 8255A.

Keyboard Status Register (KBSTAT):59H



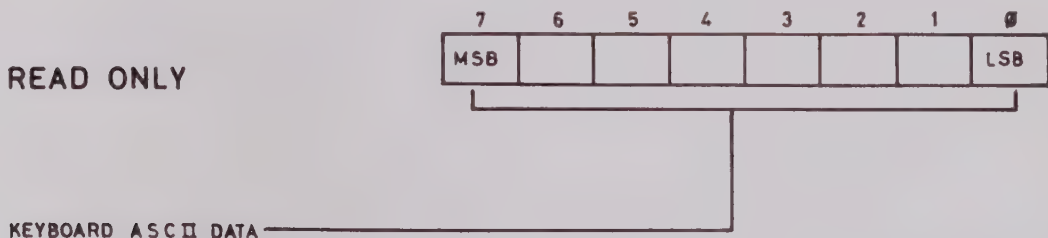
When bit 3 (Data Buffer Full) is 1 this indicates that a key has been pressed and KBDAT contains valid data, and an interrupt has been generated. Bit 3 is cleared when KBDAT is read.

When bit 4 (Interrupt Enabled) is 1 this indicates that the keyboard interrupts have been enabled.

When bit 5 (Interrupt Request) is 1 this indicates that a key has been pressed regardless of whether interrupts are enabled. Bit 5 is cleared when KBDAT is read.

Bit 0-2 and 6-7 are not used and therefore meaningless.

Keyboard Data Register (KBDAT):5BH

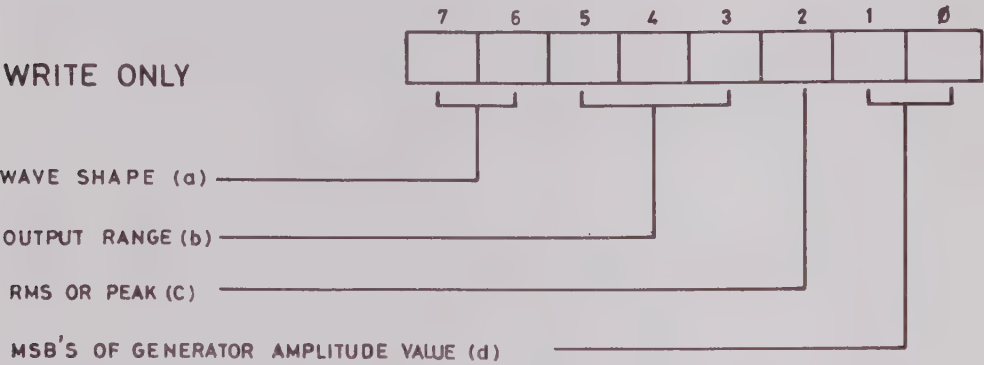


When a keyboard interrupt occurs or bit 5 of the keyboard status register is set (1), this register contains the 8-bit ASCII coded data from the keyboard. Reading this port clears bit 3 and bit 5 of the keyboard status register but the data remains valid until another key is pressed.

GENERATOR INTERFACE REGISTERS

This sub-section briefly describes and shows the bit assignments for the Generator Interface Registers.

Amplitude Register (GAM):40H



(a) Wave Shape:

Bit 7	Bit 6	Mode
0	0	Sine
0	1	Triangle
1	X	Square

Bits 6 and 7 determine the shape of the output waveform.

(X = don't care)

(b) Output Range:

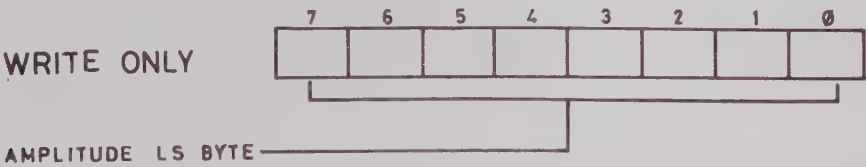
Bit 5	Bit 4	Bit 3	Range (V)
1	1	0	0.313 to 9.99
1	0	1	0.032 to 0.312
0	1	1	0.001 to 0.031

Bits 3,4 and 5 determine the range of the output voltage.

(c) Bit 2 when set (1), indicates that the output voltage is in terms of rms volts. When this bit is set to 0 the voltage is in terms of peak volts.

(d) Bits 0 and 1 represent the two most significant bits of the 10-bit fixed point binary value of the generator amplitude data.

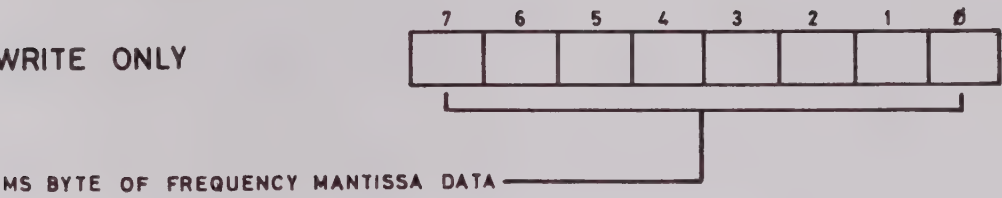
Amplitude Register (GAL):41H



Bits 0-7 represent the least significant 8 bits (byte) of the 10-bit fixed point binary value of the generator amplitude volts.

Frequency Mantissa (GFM):42H

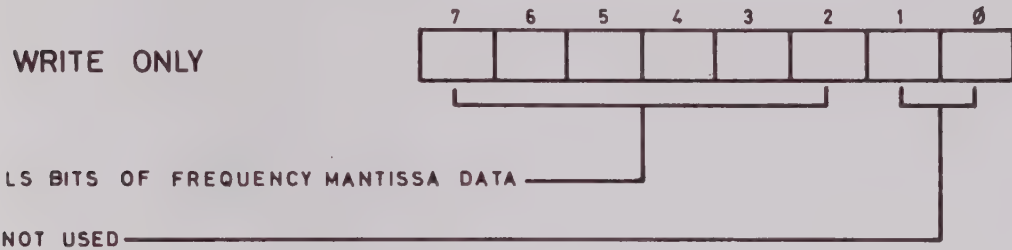
WRITE ONLY



Bits 0-7 represent the most significant 8 bits (byte) of the 14-bit Frequency Mantissa data.

Frequency Mantissa (GFL):43H

WRITE ONLY

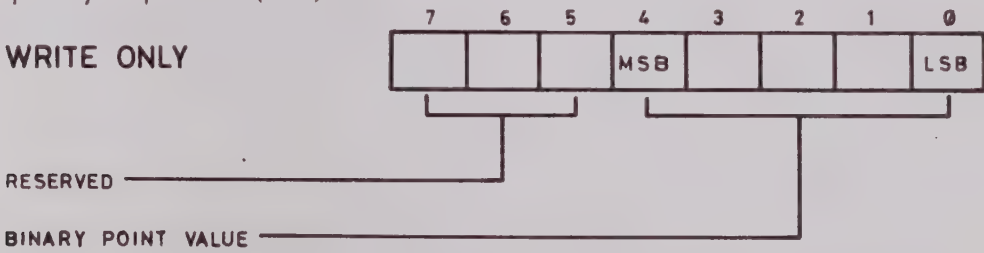


Bits 2-6 represent the least significant 6 bits of the 14-bit Frequency Mantissa data.

Bits 0-1 are not used and therefore are meaningless.

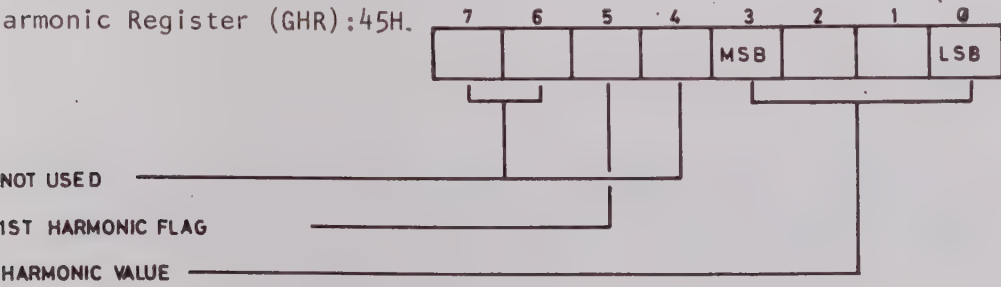
Frequency Exponent (GER):44H

WRITE ONLY



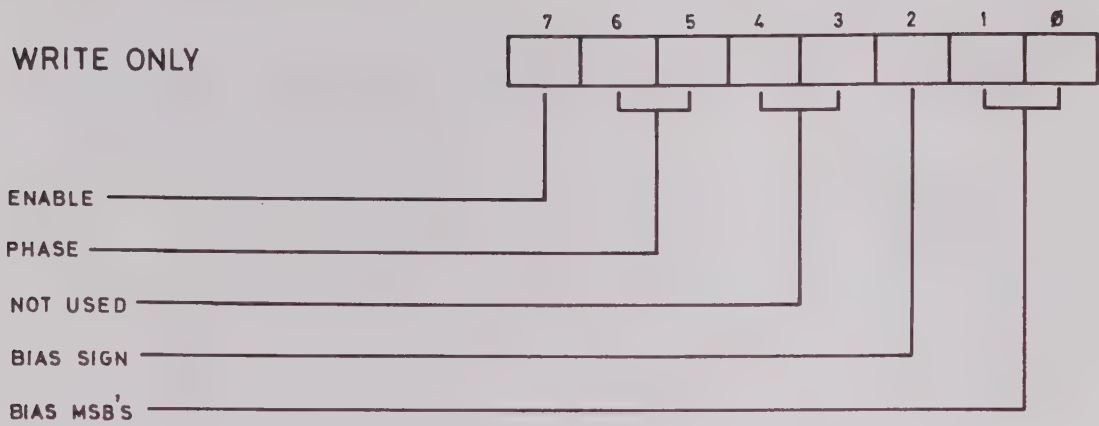
Bits 5-7 are reserved for future frequency expansion. Bits 0-4 represent the binary value of the frequency exponent.

Harmonic Register (GHR):45H.



Bits 4,6 and 7 are not used and therefore are meaningless. Bit 5 sets when the 1st. Harmonic is selected. Bits 0-3 represent the 1s complement of 1 less than the fixed point binary value of the harmonic.

End Phase (GEP):46H



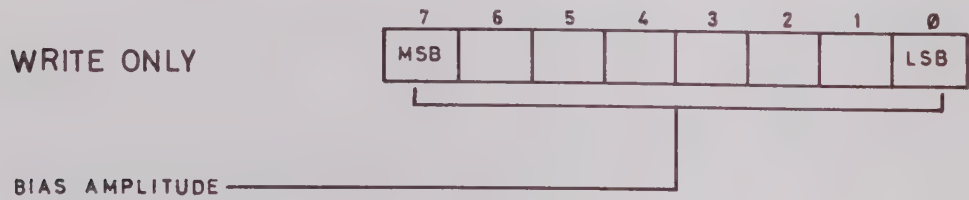
Bit 7 when set (1),causes the generator to stop at the phase specified by bits 5 and 6.

Bits 5 and 6 represent the scaled fixed point binary value of the phase, corresponding to the values from 0° to 270° in 90° steps. The bit pattern for the four phase stops are as follows:

Bit 6	Bit 5	Phase Stop
0	0	0°
1	0	90°
0	1	180°
1	1	270°

Bits 3 and 4 are not used and therefore are meaningless. Bit 2 represents the polarity of the generator bias voltage (1 = positive value and 0 = negative value). Bits 0 and 1 represent the two most significant bits of the 10-bit generator output d.c. bias value.

Bias Register (GBR):47H



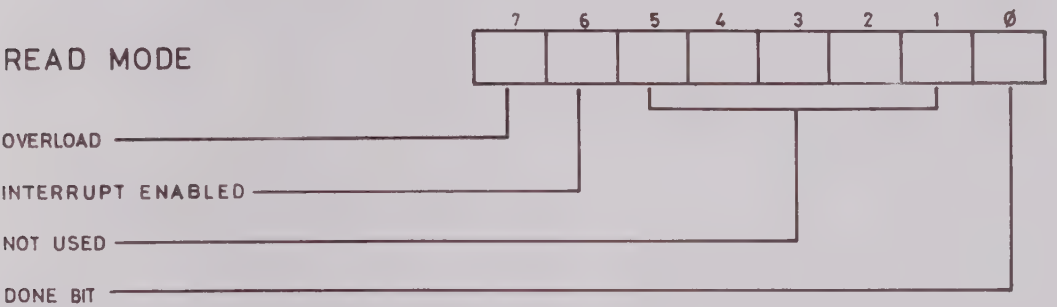
Bits 0-7 represent the 8 least significant bits of the fixed point binary magnitude of the generator output d.c. bias value,scaled to a full scale range of -9.99V to + 9.98V.

CORRELATOR INTERFACE REGISTERS

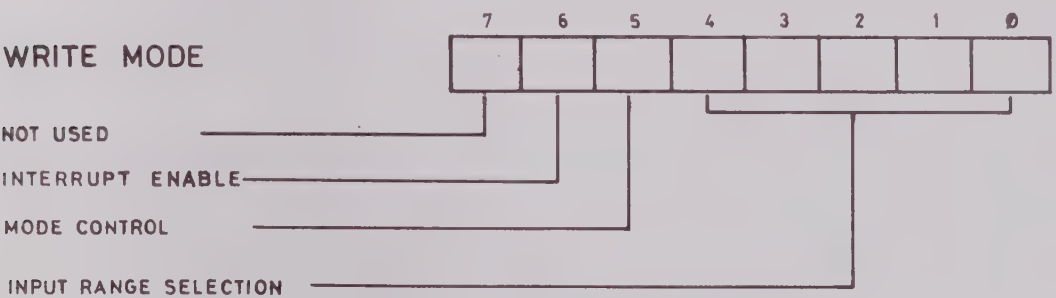
This sub-section briefly describes and shows the bit assignments for the Correlator Interface Registers. Since the FRA is designed to enable the use of two correlator channels, all registers are duplicated. Therefore, mnemonic references to registers in this sub-section are suffixed with either /1 or /2, or both, depending on whichever is applicable. When both are applicable, the associated addresses are also given respectively, e.g. (CCR1/2):48H/60H.

Command Register (CCR1/2):48H/60H

This register is both Read and Write:



Bit 7 when set (1), indicates that the correlator input circuitry is overloaded and a change of input is required. Bit 6 when set (1), indicates that correlator interrupts are enabled. Bits 1-5 are not used and therefore are meaningless. Bit 0 when set (1), indicates that the correlator has requested an interrupt which has not yet been serviced.

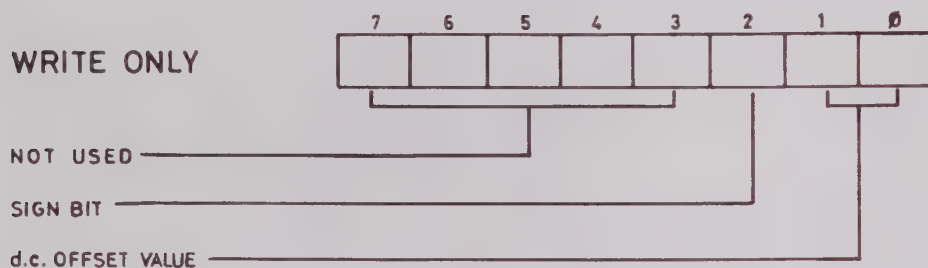


Bit 7 is not used and therefore is meaningless.
Bit 6 when set (1), enables interrupts from the correlator.
Bit 5 when set (1), puts the correlator into 'correlator mode'. When set to zero (0), it puts the correlator into 'signal averaging mode'.
Bits 0-4 are used to define the input bit pattern range selected. The bit patterns and ranges are as follows:

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Range Selected
0	*	1	0	1	0.05V
0	*	0	1	1	0.5V
1	*	0	1	1	5.0V
0	*	1	0	0	5.0V (Special)
0	*	0	1	0	50V
1	*	1	0	0	500V

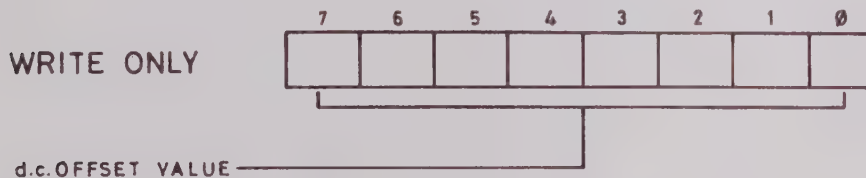
(* 1 = Peak, 0 = RMS)

Input Offset (OFFM1/2):49H/61H



Bits 3-7 are not used and therefore are meaningless. Bit 2 when set (1), represents a positive d.c. offset. When it is set zero (0), it represents a negative d.c. offset. Bits 0-1 signify the two most significant bits of the scaled 10-bit fixed point binary magnitude of the correlator input d.c. offset value.

Input Offset (OFFL1/2):4AH/62H

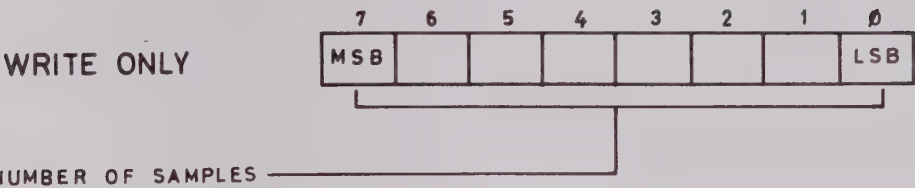


Bits 0-7 represent the 8 least significant bits (byte) of the scaled 10-bit fixed point binary magnitude of the correlator input d.c. offset value:

- ± 10V for 0.05V, 0.5V and 5V correlator ranges
- ± 1000V for 50V and 500V correlator ranges *
- ± 1000V for 5V (special) range *

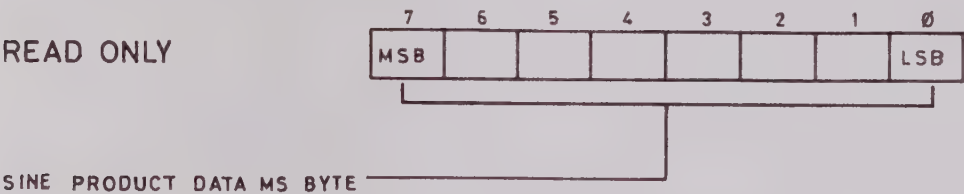
(* The maximum input voltage is 500V)

Fraction Register (CFR1/2):4BH/63H



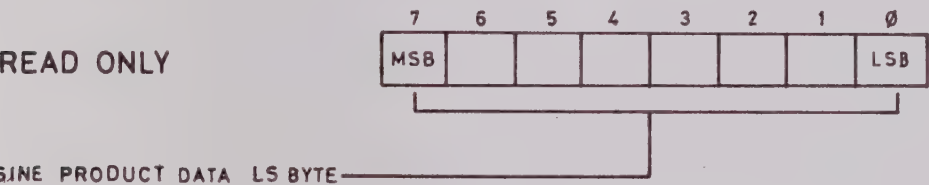
Bits 0-7 contain the number of samples required in the first block fraction input from the correlator. The number is given as a positive 8-bit binary integer.

Sine Product (CSDM1/2):4CH/64H



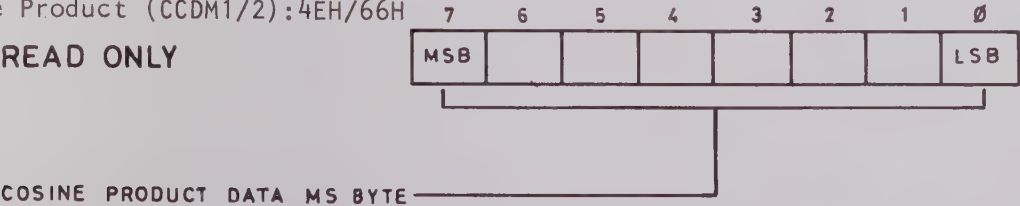
When the correlator is in the correlator mode this register contains the most significant byte of the 2s complement sine product output data. However, if the correlator is in the signal average mode the register is cleared to zero.

Sine Product (CSDL1/2):4DH/65H



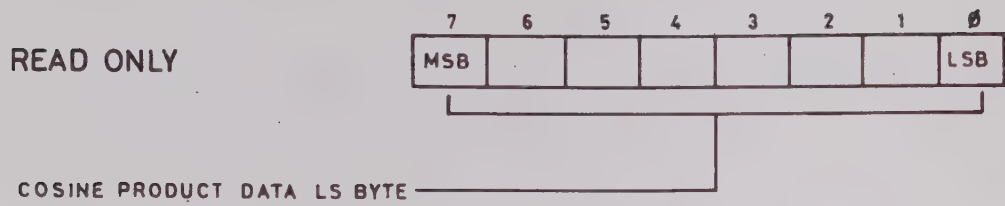
When the correlator is in the correlator mode this register contains the least significant byte of the 2s complement sine product output data. However, if the correlator is in the signal average mode the register is cleared to zero.

Cosine Product (CCDM1/2):4EH/66H



When the correlator is in the correlator mode this register contains the most significant byte of the 2s complement cosine product output data. However, if the correlator is in the signal average mode the register contains the most significant byte of the integrated sampled correlator input.

Cosine Product (CCDL1/2):4FH/67H



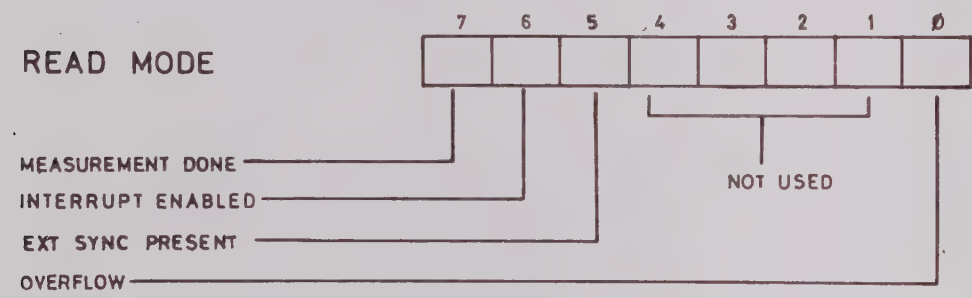
When the correlator is in the correlator mode this register contains the least significant byte of the 2s complement cosine product output data. However, if the correlator is in the signal average mode the register contains the least significant byte of the integrated sampled correlator input.

EXTERNAL SYNC REGISTERS

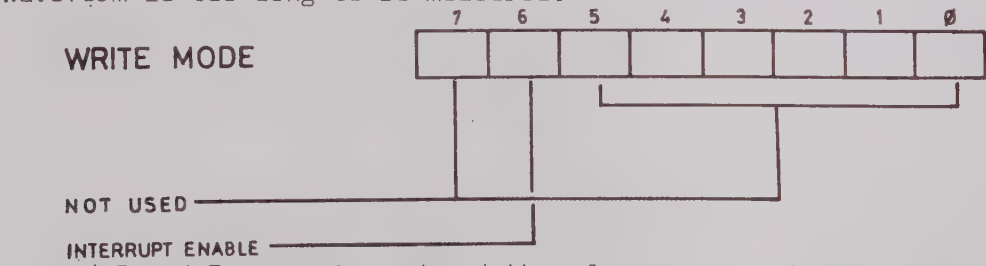
This sub-section briefly describes and shows the bit assignments for the External Sync Registers.

Command/Status Register (XSYN):50H

This register is both Read and Write.

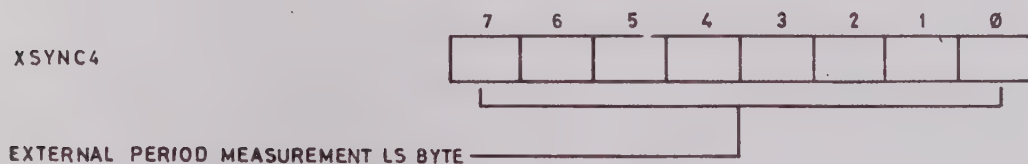
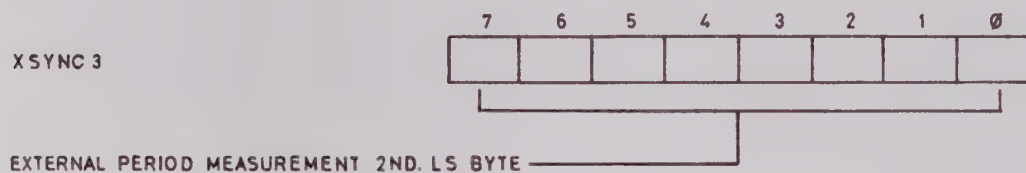
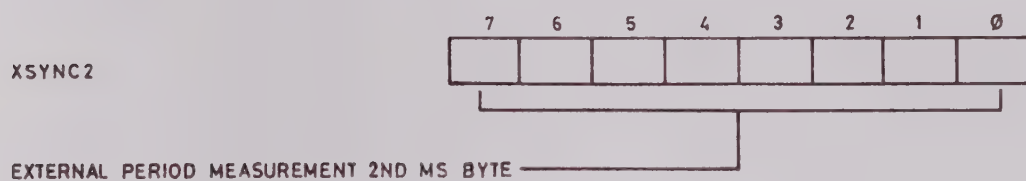
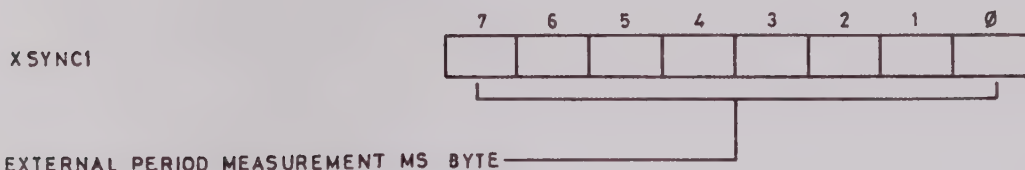


Bit 7 when set (1), indicates that the external sync has completed a measurement and also requested an interrupt. Bit 6 when set (1) indicates that the external sync interrupts are enabled. Bit 5, when set to 0 indicates external sync present. Bits 1-4 are not used and therefore are meaningless. Bit 0 when set (1) indicates that the period of the input waveform is too long to be measured.



Bits 0-5 and 7 are not used and therefore are meaningless. Bit 6 when set (1) enables the interrupts from the external synchroniser.

External Period Measurement Registers (XSYNC 1-4):54H-57H



The 4 bytes of registers XSYNC1-4 represent the 32-bit fixed point binary value of the external period measurement. The data is only valid when bit 7 (XDONE) and bit 0 (OVFL) of the command/status register (XSYN) are set to 1 and 0 respectively.

SERIAL INTERFACE REGISTERS (CCITT V24) RS232

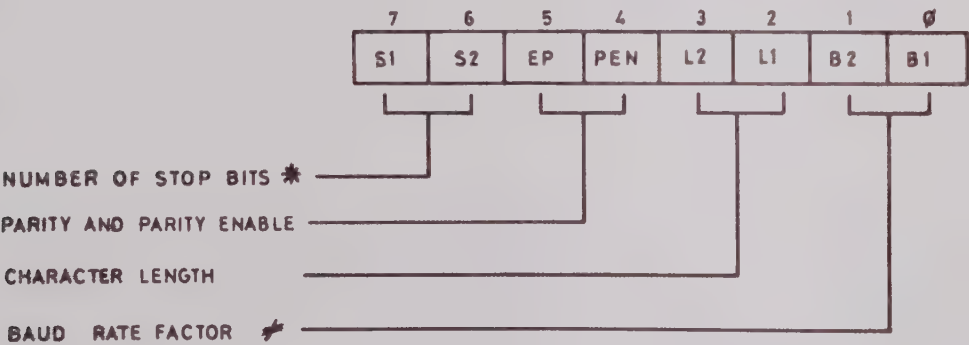
This sub-section briefly describes and shows the bit assignments for the Serial Interface Registers.

Serial Interface Control/Status Register (SICTS1):71H

This register is both Read and Write. In the Write Mode two instructions apply and they are the Mode Instruction and the Command Instruction. In the Read Mode the register bit assignments indicate the status of the device. When it is required to initialise a device, it may not be known whether the device is in the 'mode' or the 'command' format. Because of this it is recommended that a predetermined sequence of actions be followed. These actions are described under Programming Considerations.

Mode Instruction

The Mode Instruction is used to set ready for use as a device. Basically it initialises the device and sets it ready to accept a Command Instruction. The Mode Instruction must always follow a reset operation (internal or external), and once the instruction has been written, any further writes to the port are interpreted as Command Instructions. The bit assignments for the Mode Instruction are as follows:



* only affects TX-RX never requires more than 1 stop bit.

† synchronous mode is not used in this application.

Bits 6-7 specify the number of stop bits (*) required as follows:

Bit 7	Bit 6	Number of stop bits
0	0	Invalid
0	1	1
1	0	1½
1	1	2

Bit 5 indicates Parity: 1 = EVEN, 0 = ODD.
 Bit 4 indicates Parity Enable/Disable: 1 = Enable, 0 = Disable.
 Bits 2-3 specify the character length as follows:

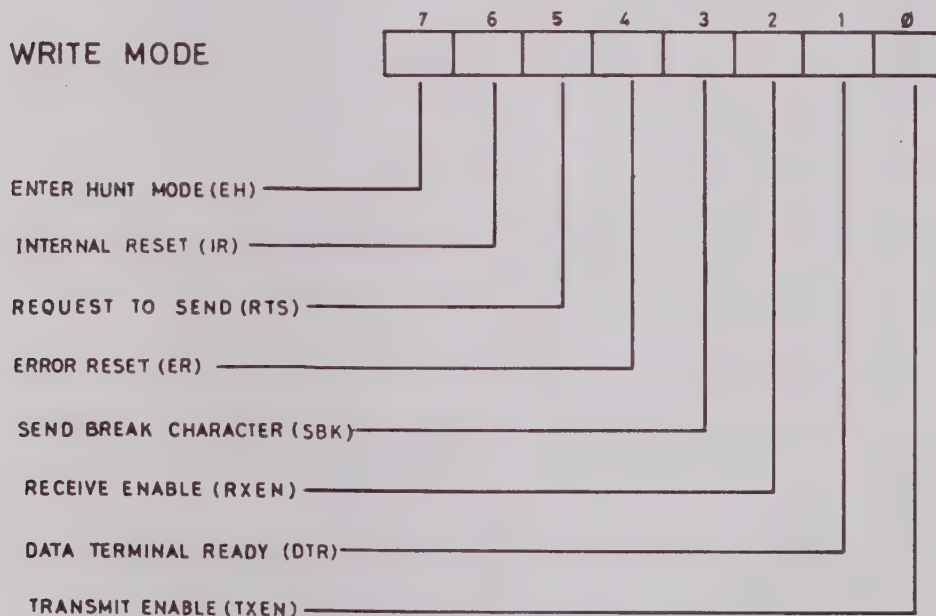
Bit 3	Bit 2	Character Length
0	0	5
0	1	6
1	0	7
1	1	8

Bits 0-1 specify the Baud Rate Factor (x) as follows:

Bit 1	Bit 0	Baud Rate Factor
0	0	Sync Mode
0	1	1x
1	0	16x
1	1	64x

Command Instruction

Once the device has been programmed by the Mode Instruction, the Command Instruction is used to control the operation. The bit assignments for the Command Instruction are as follows:

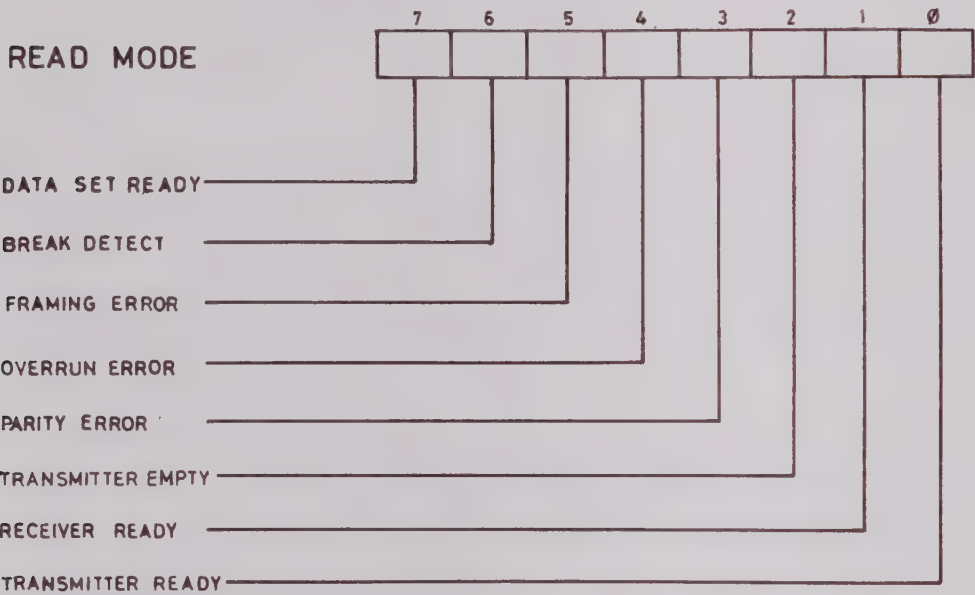


Bit 7 when set (1), enables a search for sync characters, (this is not used in the asynchronous mode).
 Bit 6 when set (1), returns the device to 'mode' instruction format.
 Bit 5 when set (1), forces the RTS output to zero.
 Bit 4 indicates Error Reset: 1 = reset error flags PE, OE and FE (bits 3,4,and 5 of Status register).
 Bit 3 when set (1), forces TX data low, 0 = normal operation.

Bit 2 enables or disables Receive: 1 = Enable, 0 = Disable.
 Bit 1 when set (1), forces $\overline{DTR}$ output to zero.
 Bit 0 enables or disables Transmit: 1 = Enable, 0 = Disable.

Whenever bit 0 or 2 of the Status register is set (1), an interrupt to the MPU is generated. To stop the receiver from generating interrupts bit 2 (Receive Enable) of the Command Instruction must be set low (0). When bit 0 (Transmit Enable) is set to 1 an interrupt is generated by bit 0 of the Status buffer, whereupon the interrupt routine then sends the first character. When the device is ready to receive each character it generates an interrupt. When the last character has been sent, bit 0 (TXEN) of the Command Instruction is set low to disable further interrupts.

Status Register



Bit 7 indicates that the $\overline{DSR}$ input pin is set low (0).
 Bit 6 when set (1) indicates a break character (all zero word - start, data, parity and one stop bit) whenever received.
 Bit 5 is set when a valid stop bit is not detected at the end of a character. This bit is reset by bit 4 of the Command Instruction and does not inhibit operation of the device.
 Bit 4 is set when the MPU fails to read a character before the next one becomes available. This bit is also reset by bit 4 of the Command Instruction and does not inhibit operation of the device, however, the previously overrun character is lost.
 Bit 3 is set when the receiver detects a parity error. This bit is also reset by bit 4 of the Command Instruction and does not inhibit operation of the device.
 Bit 2 when set indicates that the device has no characters to transmit. It is reset upon receipt of a character from the MPU (this is independent of bit 0 of the Command Instruction). The bit only goes high if the transmitter is operating below the maximum transmission rate.

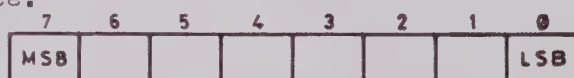
Bit 1 when set indicates that the device has a character that is ready to be input to the MPU. The bit is disabled by bit 2 of the Command Instruction when low (0).

Bit 0 indicates that the transmitter is ready to accept a data character from the MPU, and is not masked by bit 0 of the Command Instruction.

Serial Interface Data Register (SIDAT1):70H

This register is both Read and Write.

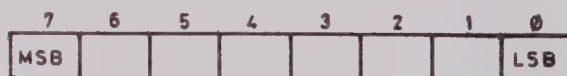
READ MODE



DATA FROM RECEIVER

When bit 1 (RXRDY) of the Status Register is set (1), this register contains valid data from the receiver. Whenever it contains a programmed character length of less than 8 bits, the LS bits represent the data and the unused bits are represented by zeros. The parity bit is not considered as a data bit when programming the word length and therefore cannot be read on the data bus.

WRITE MODE



MPU TRANSMIT DATA

When bit 0 (TXRDY) of the Status Register is set, the data to be transmitted may be written to the register by the MPU. For word lengths of less than 8 bits, the LS bits represent the data. The unused bits are 'don't care' and therefore are meaningless.

Programming Considerations

When it is required to initialise a device, it may not be known whether it is in the mode or command format. Because of this the following sequence of actions is recommended when initialising.

(a) Write 12H to SICTS1 (for Command format)

If the device is in Mode format, this Write instruction sets the asynchronous mode and passes control to the Command format.

If the device is in Command format, this Write instruction causes an error reset and the device remains in the Command format.

(b) Write 40H to SICTS1 (for Mode format)

This Write instruction causes an internal reset and control passes to the Mode format. The operating mode may now be set in accordance with the information given under *Mode Instruction* (e.g. for standard teletype, 2 stop bits, no parity, 8 data bits, Write CFH to SICTS1). When the Mode format instruction has been written, control is passed to the Command format and interrupts may be enabled or disabled for Transmit or Receive as defined under *Command Instruction*.

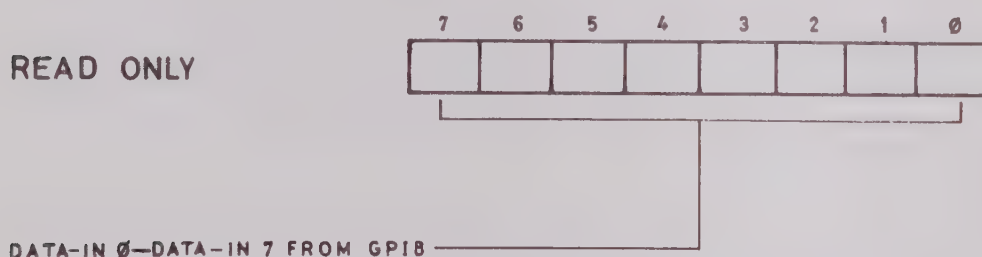
PARALLEL INTERFACE REGISTERS (IEEE 488)

This sub-section briefly describes and shows the bit assignments for the IEEE 488 Parallel Interface Registers. These registers are contained within a single Intel 8291 chip. This device, together with the addition of Driver/Receiver, Address selection logic, and a latch for reading the General Purpose Interface Bus (GPIB) address, Talk Only/Listen Only, and Return to Local Status handles the IEEE 488 interface.

In order to drive the device it must first be 'initialised' into an operating mode. This is implemented by loading the various registers with the data required for the mode of operation desired. The device has 8 'read' registers and 8 'write' registers which are accessed by selecting the 'Register Select Code' (RS0-RS2) with either $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ to the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ inputs.

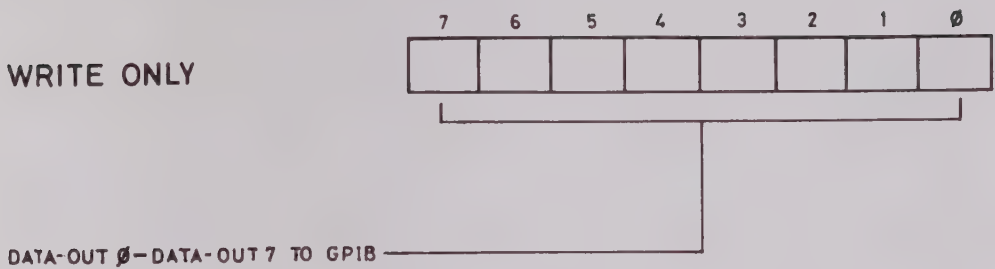
Data-In (Read)/Data-Out (Write) Registers

Data-In Register (DATIN): 30H



This register is used to move data from the GPIB to the microprocessor or to memory when the device (8291) is addressed to listen. Incoming information is separately latched by the register, and its contents are not destroyed by a write to the 'Data-Out Register'. The RFD (Ready for Data) message is held false until the byte is removed from the 'Data-In Register', either by the microprocessor or by DMA. The 8291 then completes the handshake automatically. In RFD/DAV holdoff mode (see Auxiliary Register 'A'), the handshake is not completed until a command is sent telling the 8291 to release the holdoff. In this way, the same byte may be read several times, or an over anxious talker may be held off until all available data has been processed.

Data-Out Register (DATOUT):30H



When the device (8291) is addressed to talk, it uses this register to move data onto the GPIB. Upon a write to this register, the 8291 initiates and completes the handshake by sending the byte out over the bus. When the RFD/DAV is in effect, data is held until the release command is issued. A read of the 'Data-In Register' does not destroy the information in the 'Data-Out Register'.

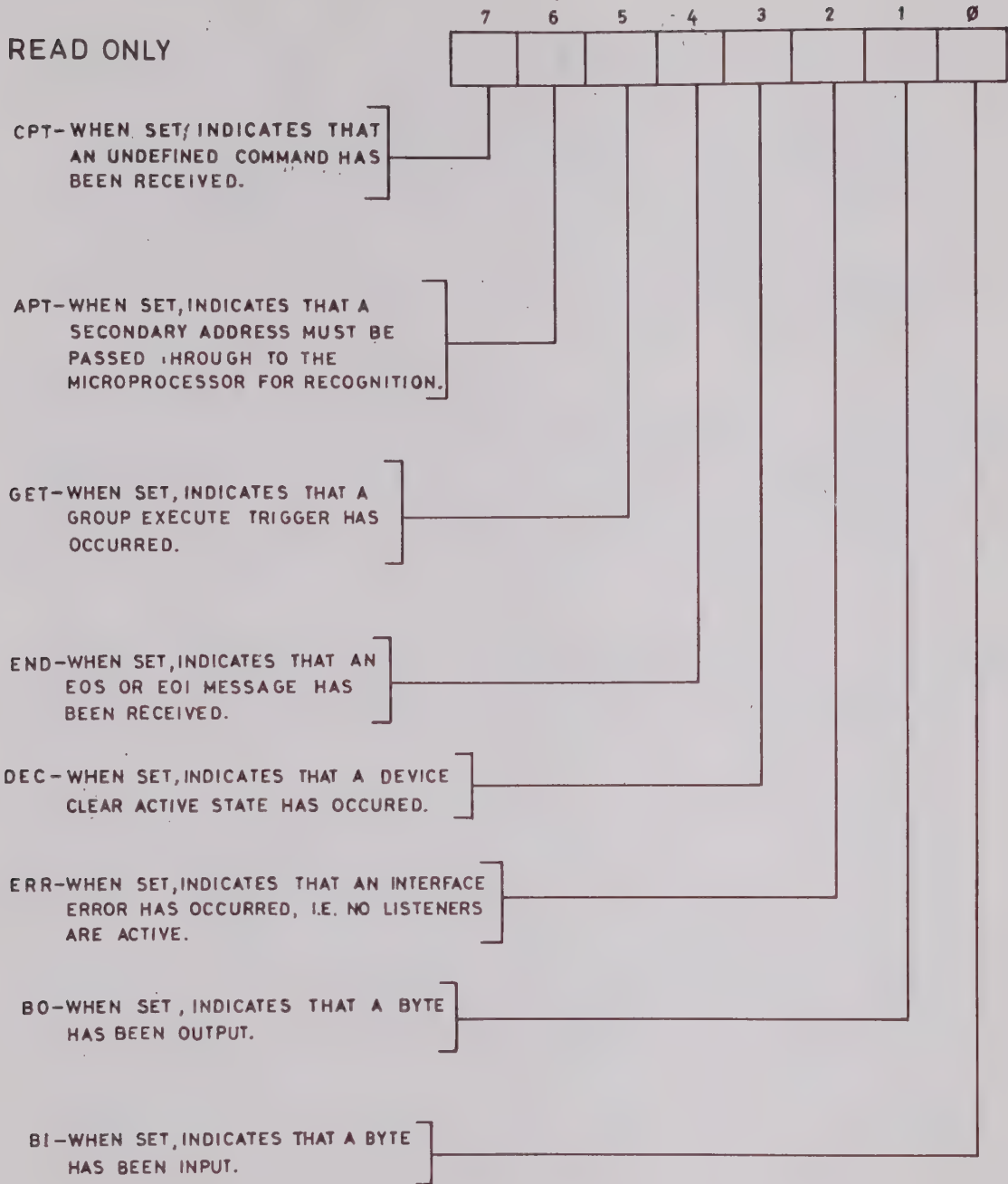
INTERRUPT STATUS/MASK REGISTERS

There are 4 interrupt registers, viz. Interrupt Status 1, Interrupt Status 2, Interrupt Mask 1 and Interrupt Mask 2 and the occurrence of any one of 12 conditions or events on the GPIB will generate an interrupt to the microprocessor.

Upon the receipt of an interrupt, the microprocessor reads the Interrupt Status Registers to determine which event has occurred and then it executes the appropriate service routine (if applicable). Each status register has an associated mask register, thus each of the 12 interrupt status bits has a matching mask bit. The mask bits are used to select the events that will cause the INT pin to be asserted. Writing a '1' into any of these bits enables the corresponding interrupt status bits to generate an interrupt. The bits in the Interrupt Status Registers are set regardless of the state of the matching bits in the Mask Registers. Upon being read or when a local power-on (pon) message is executed, the Status Registers are cleared. If an event occurs while one of the Status Registers is being read, that event is held until after its register is cleared and then it is placed in the register. The bit assignments for each register is given in the following sub-sections.

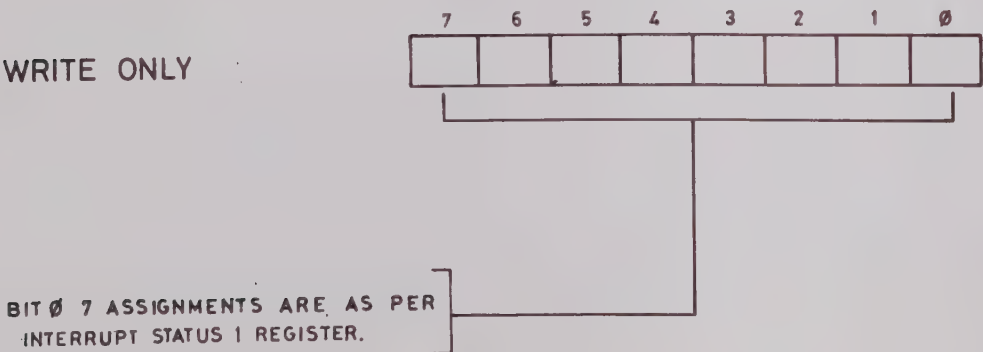
Interrupt Status 1 Register (INTS1):31H

READ ONLY



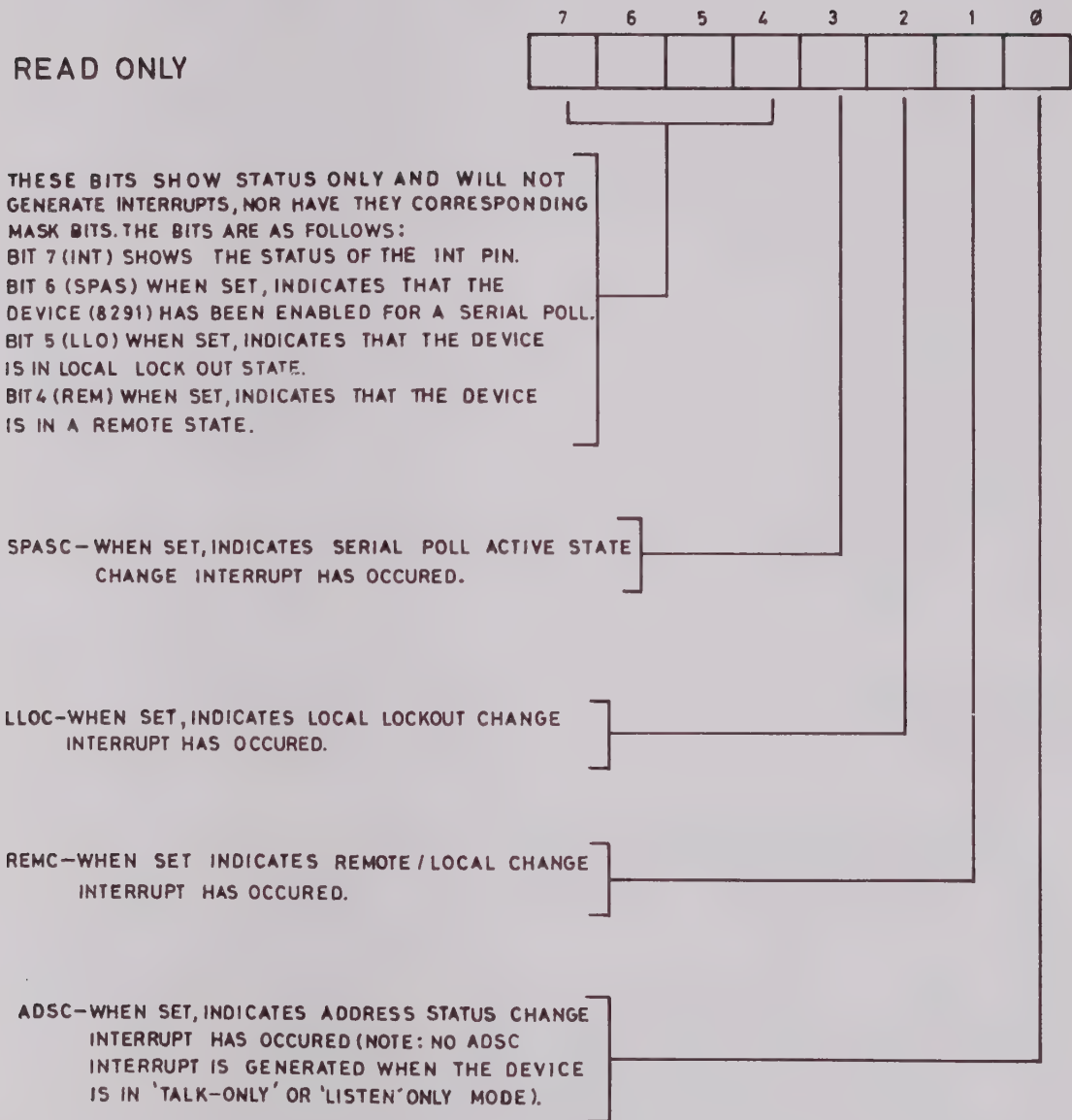
Interrupt Mask 1 Register (INTM1):31H

WRITE ONLY

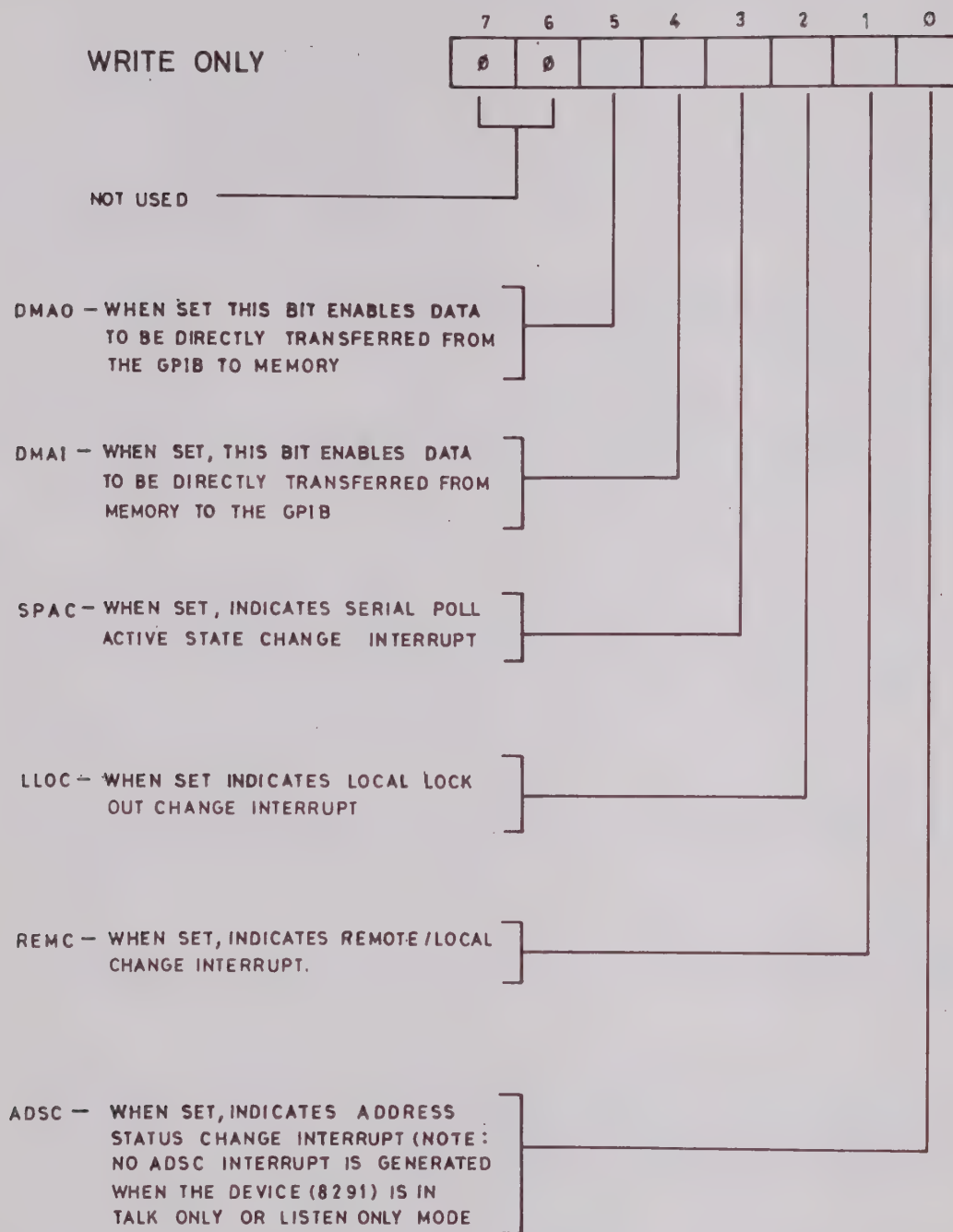


Interrupt Status 2 Register (INTS2):32H

READ ONLY



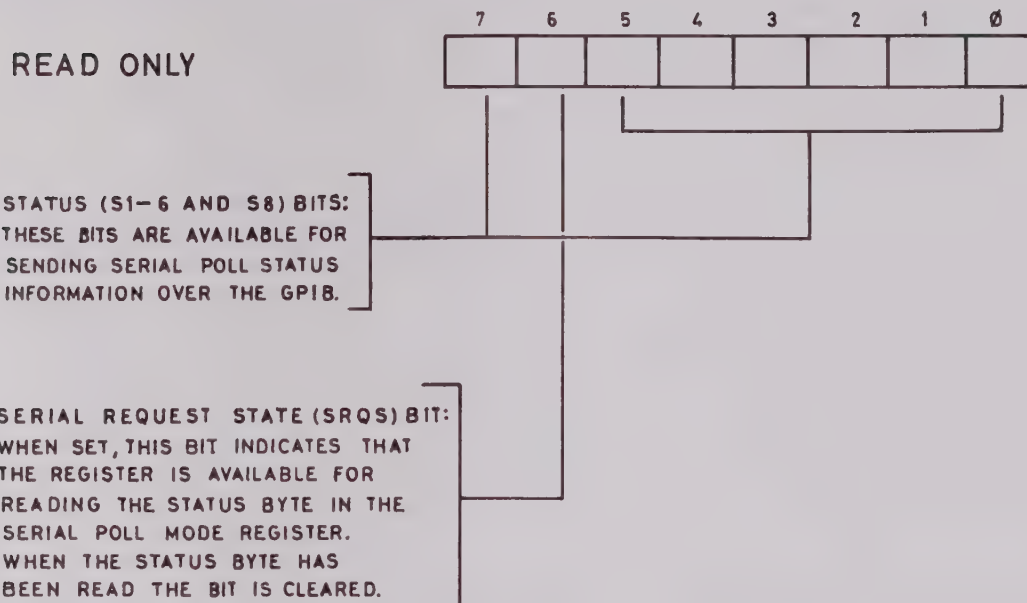
Interrupt Mask 2 Register (INTM2):32H



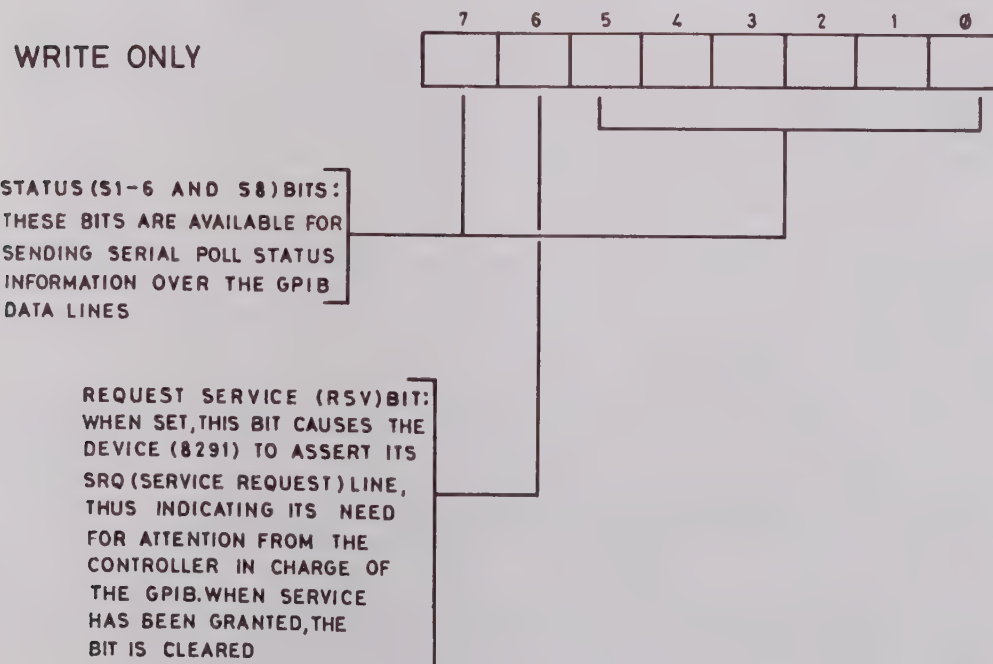
Serial Poll Status and Mode Registers

The Serial Poll Status Register is available for reading the status byte in the Serial Poll Mode Register. The Serial Poll Mode Register is used to establish the status byte that the device (8291) sends out on the GPIB data lines when it receives the SPE (Serial Poll Enable) message.

Serial Poll Status Register (SPS):33H



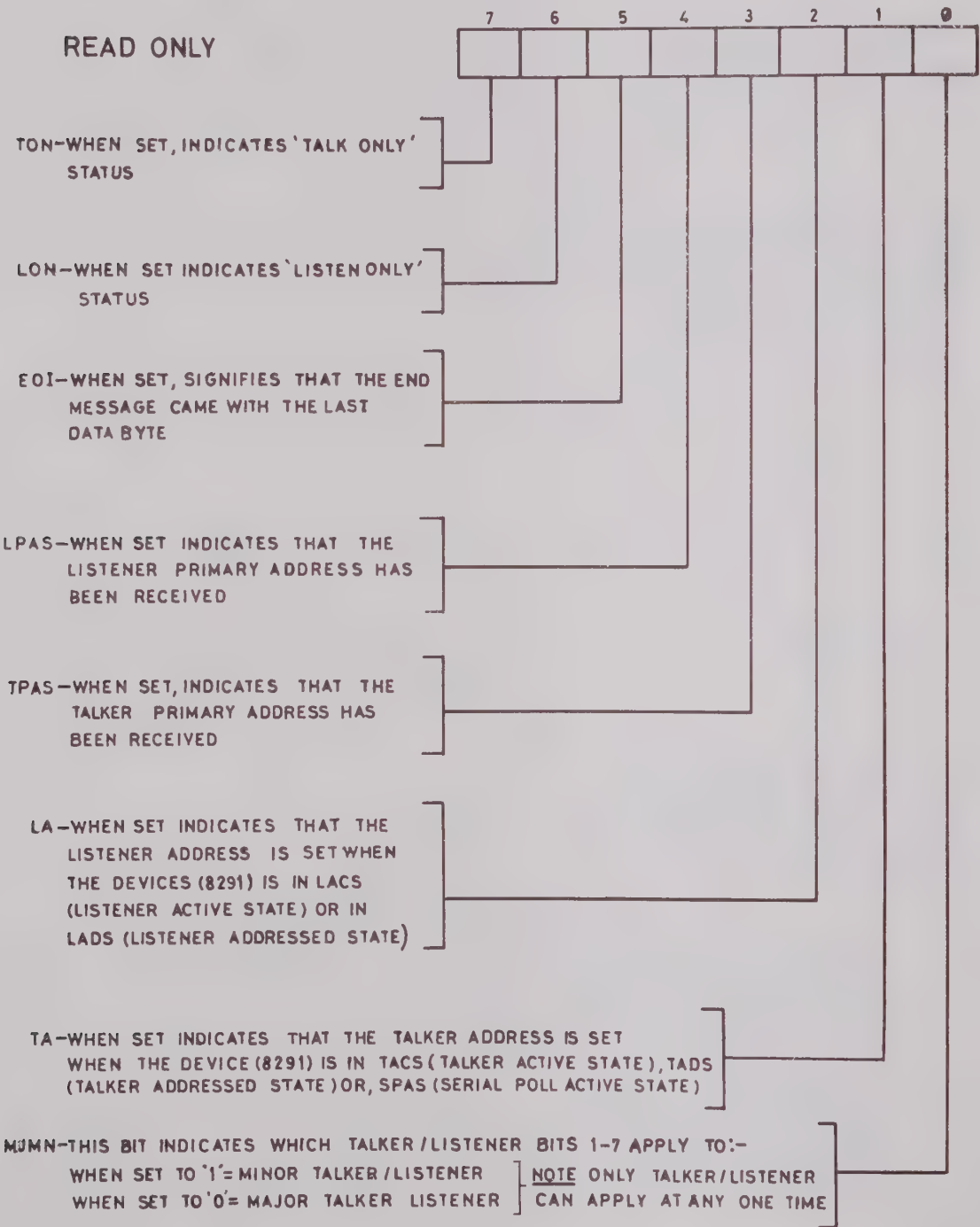
Serial Poll Mode Register (SPM):33H



Address Status and Mode Registers

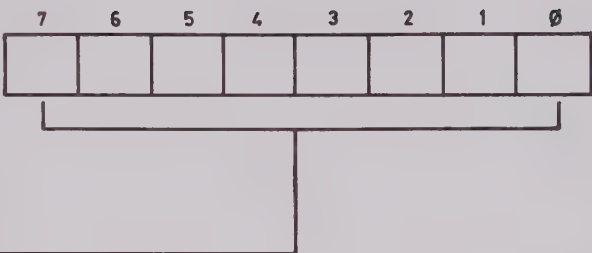
The Address Status Register contains information used by the micro-processor to handle its own addressing. The Address Mode Register is used to select one of the five modes of addressing available on the 8291 device. It determines the manner in which the device uses the information in the Address 0 and Address 1 Registers.

Address Status Register (ADDRS):34H



Address Mode Register (ADDRM):34H

WRITE ONLY



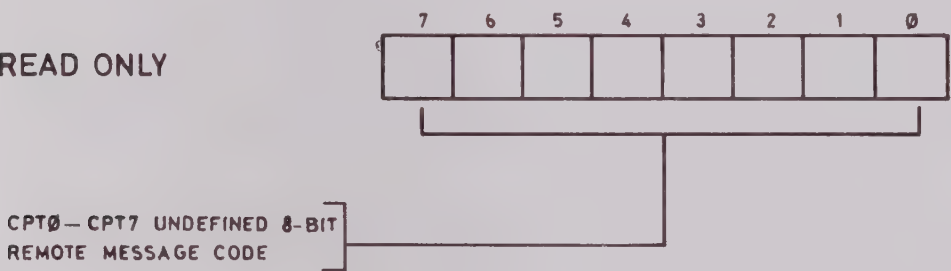
The mode of addressing implemented by the device (8291) may be selected by writing one of the following bytes:

Register Contents (byte)	Addressing Mode
1 0 0 0 0 0 0 0	Enable talk only mode (ton)
0 1 0 0 0 0 0 0	Enable listen only mode (lon)
1 1 0 0 0 0 0 0	The device may talk to itself
0 0 0 0 0 0 0 1	Mode 1, (Primary-Primary)
0 0 0 0 0 0 1 0	Mode 2, (Primary-Secondary)
0 0 0 0 0 0 1 1	Mode 3, (Primary/APT-Primary/APT)

NOTE: The Address Mode Register determines the way in which the 8291 device uses the information in the 'Address 0' and 'Address 1' Registers.

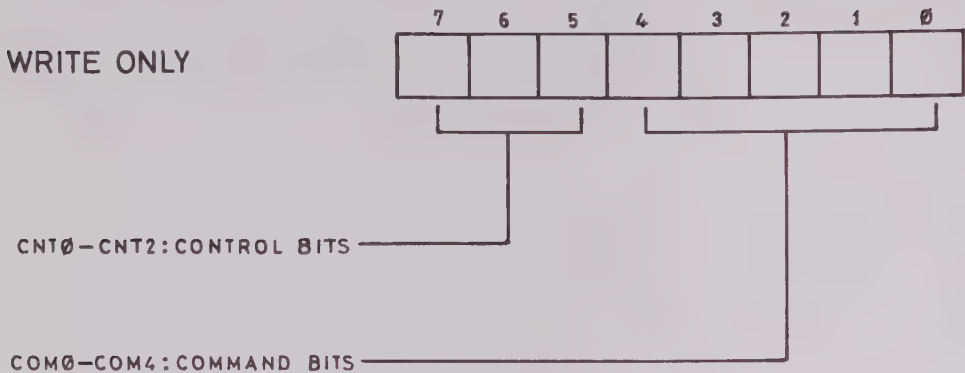
Command Pass Through Register (CPT):35H

READ ONLY



The Command Pass Through Register is used to transfer undefined 8-bit remote message codes from the GPIB to the microprocessor. When the CPT feature is enabled, i.e. bit 0 of the Auxiliary Register B set, any message not decoded by the device (8291) becomes an undefined command. When Mode 3 addressing is used, secondary addresses are passed through the CPT Register. In either case, the device will hold off the handshake until the microprocessor reads this register and issues the VSCMD (Non-Valid/Valid Secondary Address/Command) auxiliary command.

Auxiliary Mode Register (AUXMOD):35H



The three-bit control field (CNT0-CNT2) and the five-bit command field (COM0-COM4) are used for the following purposes:

- (a) To load 'hidden' auxiliary registers (A and B) on the 8291 device.
- (b) To issue commands from the microprocessor to the 8291 device.
- (c) To preset an internal counter used to generate T1 delay in the source handshake function.

The following table summarises how the above tasks are performed with the Auxiliary Mode Register. Note that the three control bits determine how the five command bits are interpreted.

CODE			COMMAND				
Control Bits	Command Bits						
0 0 0	0	C C C C	Execute auxiliary command CCCC.				
0 0 1	0	F F F F	Preset internal counter to match external clock frequency of FFFF MHz (FFFF= binary representation of 1 to 8 MHz).				
1 0 0	D ₄	D ₃ D ₂ D ₁ D ₀	Write data D ₄ D ₃ D ₂ D ₁ D ₀ into Auxiliary Register A.				
1 0 1	0	D ₃ D ₂ D ₁ D ₀	Write data D ₃ D ₂ D ₁ D ₀ into Auxiliary Register B.				
0 1 1	U	SP ₃ P ₂ P ₁	Configure/inconfigure parallel poll SP ₃ P ₂ P ₂ as defined in Std.488 Configure if U = 0, unconfigure if U = 1. This command is the local poll enable (lpe) message when U = 0.				

Auxiliary Commands

Auxiliary commands are executed by the 8291 device whenever 0 0 0 0 C C C C is written into the Auxiliary Mode Register, where C C C C is the 4-bit command code. The commands associated with this 4-bit code are as follows:

4-BIT CODE	COMMAND
0 0 0 0	Immediate Execute pon
0 0 1 0	Chip Reset (initialise)
0 0 1 1	Finish Handshake
0 1 0 0	Trigger (GET command)
0 1 0 1	Return to Local
0 1 1 0	Send EOI
0 1 1 1	Invalid Secondary Address/Command received
1 1 1 1	Valid Secondary Address/Command received
1 0 0 1	Clear Parallel Poll Flag
0 0 0 1	Set Parallel Poll Flag

Auxiliary Register A

This is a 'hidden' five-bit register which is used to enable some of the 8291 device features. Whenever a 1 0 0 D₄ D₃ D₂ D₁ D₀ byte is written to the Auxiliary Mode Register, it is loaded with the data D₄ D₃ D₂ D₁ D₀. Setting the respective bits enables the following features:

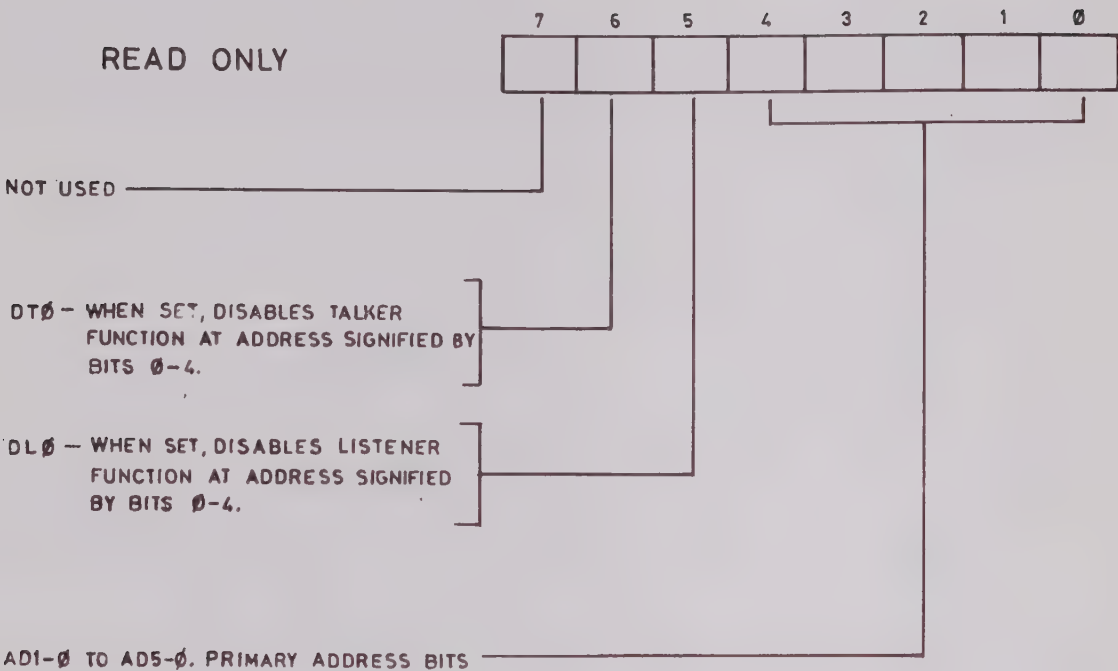
- D₀ (Bit 0) - RFD/DAV holdoff on all Data
- D₁ (Bit 1) - RFD/DAV holdoff on End
- D₂ (Bit 2) - End on EOS Received
- D₃ (Bit 1) - Output EOI on EOS Sent
- D₄ (Bit 4) - EOS Binary Compare

Auxiliary Register B

This is a 'hidden' 4-bit register which is used to enable some of the features of the 8291 device. Whenever a 1 0 1 0 D₃ D₂ D₁ D₀ is written into the Auxiliary Mode Register, it is loaded with the data D₃ D₂ D₁ D₀. Setting the respective bits enables the following features:

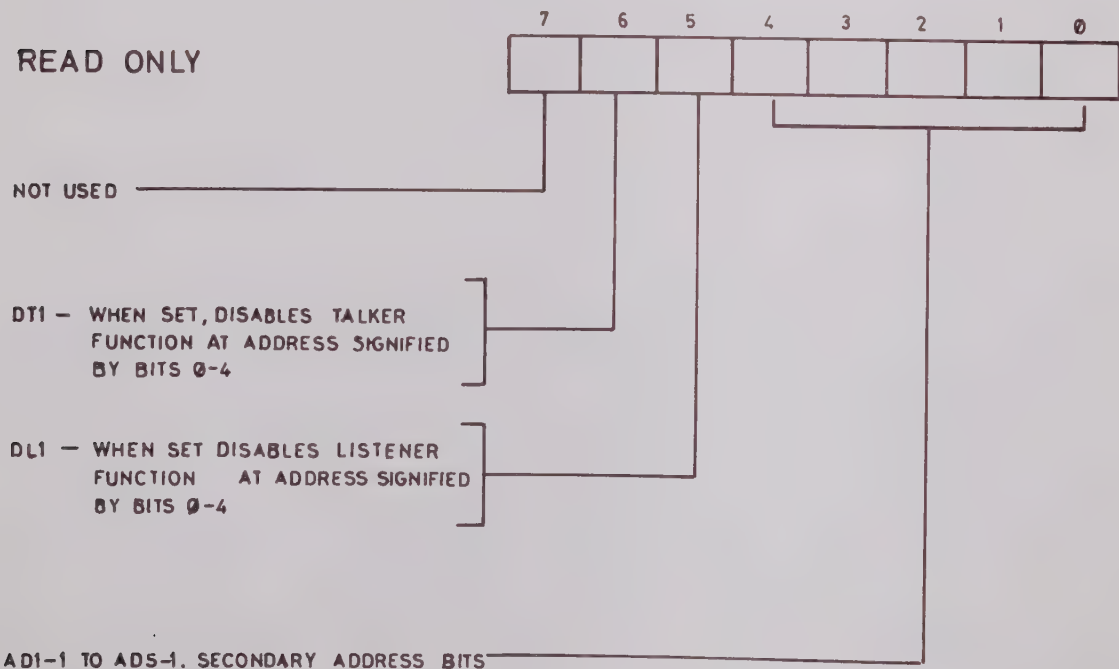
- D₀ (Bit 0) - Enable Undefined Command Pass Through
- D₁ (Bit 1) - Send EOI in SPAS (Special Poll Active State)
- D₂ (Bit 2) - Enable High Speed Data Transfer
- D₃ (Bit 3) - Enable Active Low Interrupt

Address 0 Register (ADDR0):36H



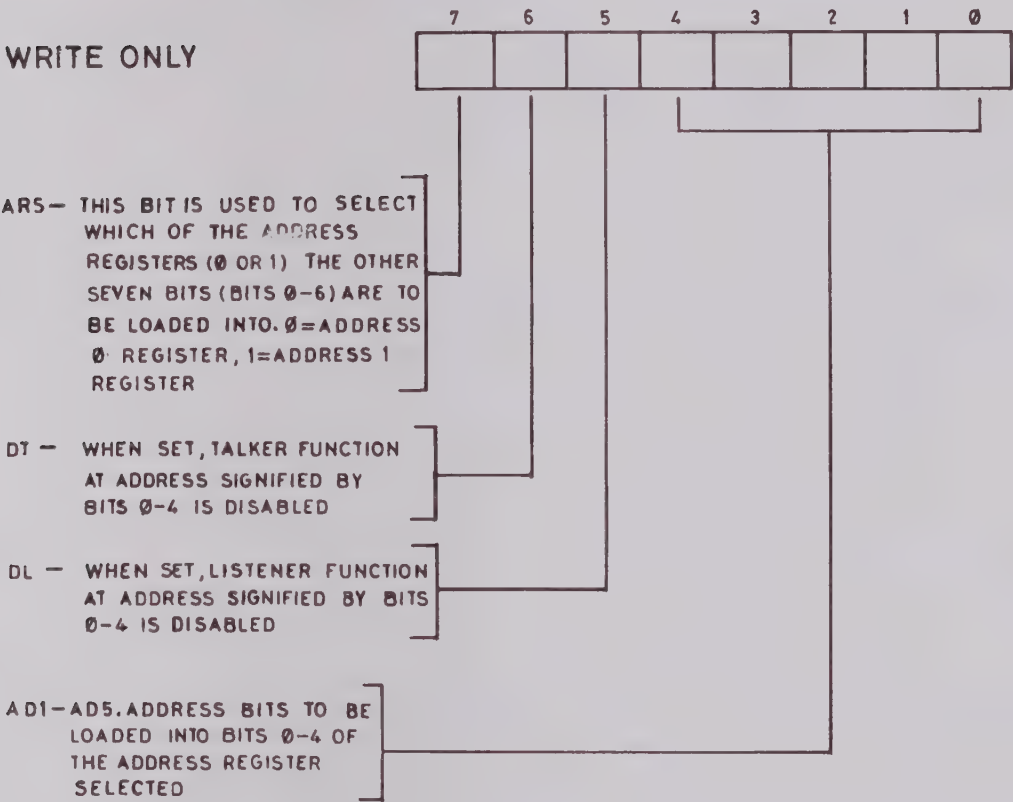
This register is one of a pair which is used by the Address Mode Register for storing the primary address when two addresses are needed by the 8291 device. The register is loaded from the Address Mode Register under control of the Address 0/1 Register.

Address 1 Register (ADDR1):37H



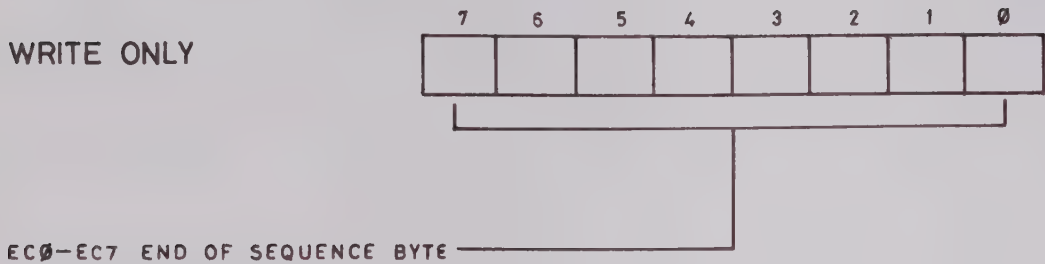
This register is one of a pair which is used by the Address Mode Register for storing the secondary address when two addresses are needed by the 8291 device. The register is loaded from the Address Mode Register under control of the Address 0/1 Register.

Address 0/1 Register (ADDR0/1):36H



This register is used for specifying the device's (8291) addresses according to the format selected in the Address Mode Register. The five-bit addresses may be loaded into the Address 0 and Address 1 registers by writing into the Address 0/1 Register.

End of Sequence Register (EOS):37H

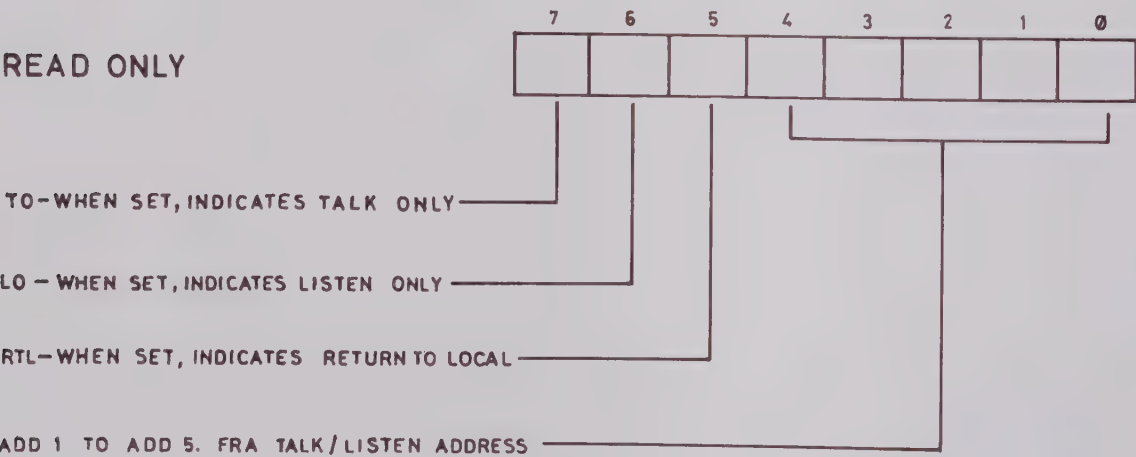


This register and its features offer an alternative to the 'Send EOI' auxiliary command used by the Auxiliary Mode Register. A seven or eight bit byte (ASCII or binary) may be placed in the register to flag the end of block or end of read. The type of EOS byte to be used is selected by bit D₄ of the Auxiliary Register A.

If the 8291 device is a listener, and the 'End on EOS Received' is enabled at bit D₂ of Auxiliary Register A, then an End interrupt is generated in the Interrupt Status 1 Register whenever the byte in the Data-In Register matches the byte in the EOS Register.

If the 8291 device is a talker, and the 'Output EOI on EOS Sent' is enabled at bit D₃ of the Auxiliary Register A, then the EOI line is sent true with the next data byte whenever the contents of the Data-Out Register matches the EOS Register.

Bus Address Register (BADDR):38H



SECTION 6

CIRCUIT DESCRIPTIONS

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Correlator Control Board	Chapter 6.5	6.5.1
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NOTE TO READERS

The following p.c. boards are contained in their relevant options manuals:

Communications & G.P.I.B. Board
External Sync I/P Unit
External Sync Control Board
Graphics Control Board

PROCESSOR AND CURSOR CONTROL BOARD

CHAPTER 6.1

Introduction

The Processor and Cursor Control Board is the heart of the F.R.A. system, controlling the sequence of functions performed, the display, and a considerable proportion of the arithmetic processing.

An overall functional block diagram of the board is given in fig. 6.1.9. Detailed functional diagrams of individual sections of the board circuits are given as indicated in the descriptions which follow.

MICROPROCESSOR (fig. 6.1.1)

The Microprocessor is implemented by means of devices which are specifically intended for microcomputer applications. These are complex devices, and a detailed discussion of their design and operation is beyond the scope of this handbook. This section therefore confines itself to summarising the facilities which each of the devices provides, the part that the Microprocessor plays in the overall functioning of the board being outlined in later paragraphs. For complete information regarding any of the devices, reference should be made to the manufacturer's documentation.*

Clock Generator and Driver

The crystal-controlled Clock Generator and Driver provides the two-phase clocking arrangement required by the Processor, together with a number of auxiliary functions and timing signals, as described below.

OSC (OSCILLATOR OUTPUT). This is a TTL-compatible signal at the crystal frequency of 18.432 MHz.

$\Phi 1$, $\Phi 2$. These are the two clock signals that are developed specifically for use by the Processor. Their timing relationship is illustrated in fig. 6.1.2.

$\Phi 2(TTL)$. This is a TTL-compatible $\Phi 2$ signal that is used to clock devices on the board, and elsewhere in the system, which are associated with D.M.A. activities.

* 8080 Microcomputer Systems User's Manual

Obtainable from: Literature Department,
Intel Corporation (UK) Ltd.,
Broadfield House,
4 Between Towns Road,
Cowley, Oxford OX4 3NB
Tel: (0865) 711829

RESET. Immediately following the application of power to the system, the voltage at the RESIN (RESET INPUT) terminal of the Clock Generator and Driver commences to rise from the logic low level towards the logic high level, at a rate controlled by the Reset Delay. Some 614 ms after power on, the voltage passes through the logic high threshold, and on the next rising edge of $\Phi 2$ the generator responds to the input by making its RESET output signal high for a minimum of three $\Phi 2$ periods. This causes the Processor to be reset, various other devices within the board to be reset, and an INTL (INITIALISE) pulse to be passed to other areas of the F.R.A.

STSTB (STATUS STROBE). The STSTB output is obtained by gating the SYNC pulse input from the Processor, initiated by the first rising edge of $\Phi 2$ in each machine cycle, with an internally-derived timing signal. This results in a narrow logic low pulse occurring at the earliest possible moment in the cycle at which the status data output of the Processor can be stable.

READY. The READY signal indicates to the Processor that valid memory or input data is available on the Processor Data Bus. If after issuing an address the Processor does not receive a READY input, it enters a WAIT state for as long as the READY line is low. In this way, the operation of the Processor can be synchronised with that of slower memory or I/O devices.

The F.R.A. memory is fast enough for the WAIT state not to be required. Hence normally the READY signal is held high by the permanent high applied at the RDYIN (READY INPUT) terminal of the generator. However, when the F.R.A. is used with an In-Circuit Emulator (I.C.E.), the link LK2 is set to the I position. This brings the READY signal under the control of the LSL (LINE STORE LOAD) signal generated by Display Control Board 2, causing the Processor to be set to the WAIT state for the duration of the display line refresh period.

Processor

The Processor takes the form of a complete, 8-bit parallel, central processing unit contained in a single integrated circuit. Separate 16-bit address and 8-bit bidirectional data busses are used to facilitate interfacing with the memory and the peripheral devices, the signals required for the control of the interfaces being generated directly by the Processor. Provision is made for a direct memory access (D.M.A.) mode of working. A brief description of each of the processor functions is given in the subsections which follow.

A0-A15 (ADDRESS BUS). The tristate ADDRESS BUS provides the address to memory or indicates the vector and port address of the peripheral device. A0 is the least significant address bit.

D0-D7 (DATA BUS). This tristate bus provides bidirectional communication between the Processor and the System Controller for instructions and data transfers. Also, during the first clock period of each machine cycle it carries a status word which describes the current machine cycle. D0 is the least significant data bit.

SYNC. (SYNCHRONISING SIGNAL). The SYNC signal is generated to indicate the start of each machine cycle.

DBIN (DATA BUS IN). The DBIN signal indicates to external circuits that the Processor Data Bus is in the input mode.

READY. See Clock Generator and Driver.

WAIT. The WAIT signal acknowledges that the Processor is in the WAIT state. It is not used in the present application.

$\overline{WR}$ ($\overline{WRITE}$). This output signal is used for memory and peripheral control during processor WRITE instructions. The data on the Processor Data Bus is stable while $\overline{WR}$ is active (low).

HOLD. The HOLD signal requests the Processor to enter the HOLD state. This state allows an external device to gain control of the System Address and Data Busses as soon as the use of the busses in the current machine cycle is completed. As a result of the Processor entering the state, the processor busses are set to the high impedance state.

HLDA (HOLD ACKNOWLEDGE). The HLDA signal appears in response to the HOLD signal and indicates that the Processor Data and Address Busses will go to the high impedance state.

INTE (INTERRUPT ENABLE). This signal is set high to indicate that the Processor will accept interrupts. It can be set and reset by program, and is automatically reset when an interrupt is accepted and when a RESET signal is applied to the Processor. Any instruction in progress is completed before the interrupt is processed.

INT (INTERRUPT REQUEST). The Processor recognises an interrupt request on this line at the end of the current instruction or while halted. If the Processor is in the HOLD state or INTE is low, the request is not honoured.

RESET. On application of a RESET signal (generated as described earlier) the program counter, and INTE and HLDA signals, are reset; also, the status is set to indicate an 'instruction fetch'. Thus the program commences with an instruction fetch being performed at location 0 in the memory.

$\Phi 1, \Phi 2$. This is the two-phase clocking required by the Processor and generated by the Clock Generator and Driver. The signals are not TTL compatible.

Timing. The basic instruction cycle timing is illustrated in fig. 6.1.3.

System Controller and Data Bus Driver

The System Controller and Data Bus Driver generates all the control signals required to directly interface the Processor with the memory and the peripheral devices, and also provides buffering between the Processor Data Bus and the System Data Bus. The main functions of the element are summarised below.

Bidirectional Bus Driver. An 8-bit, bidirectional bus driver is provided to buffer the Processor Data Bus from the memory and the peripheral devices. The driver is controlled by internally-derived signals such that proper bus flow is maintained and its outputs can be forced into the high impedance state for D.M.A. activities.

STSTB (STATUS STROBE). On application of a STSTB pulse (see Clock Generator and Driver) the current status information is latched into the Controller.

MEMR (MEMORY READ), IOR (INPUT OUTPUT READ), INTA (INTERRUPT ACKNOWLEDGE). These 'read' control signals are derived by suitably gating the appropriate status bits with the DBIN input from the Processor.

MEMW (MEMORY WRITE), IOW (INPUT OUTPUT WRITE). These 'write' control signals are derived by suitably gating the appropriate status bits with the WR input from the Processor.

BUSEN (BUS ENABLE). This is an asynchronous input which enables/disables the Controller. With the signal high, the data bus and control signal outputs are held in the high impedance state. When it is low, normal controller operation is enabled.

INTA (INTERRUPT ACKNOWLEDGE). The INTA signal is generated in response to interrupt acknowledge status and DBIN active inputs from the Processor. It is used to gate the interrupt instruction port onto the data bus.

Timing. Typical controller waveform timing is shown in fig. 6.1.4.

OPERATION

System Clock Generation (fig. 6.1.9)

The 18.432 MHz OSC output of the Clock Generator and Driver is divided by three to produce the system clock, $\Phi 3$. On each falling edge of $\Phi 2$ (TTL), the $\Phi 3$ Clock Sync. Generator produces a pulse output which causes $\Phi 3$ to be preset high; this ensures that $\Phi 3$ is maintained in synchronism with $\Phi 2$ (TTL), as shown in fig. 6.1.2.

Memory Read (fig. 6.1.1)

The Microprocessor performs a memory read:

- (1) As the first machine cycle of any program, to fetch the first instruction from memory.
- (2) As the first machine cycle of each subsequent instruction cycle, to fetch the current instruction from memory.
- (3) Whenever an instruction requires data to be read from memory.

The read commences with the Processor placing on its address bus the address of the memory location at which the read is to be performed and outputting 'instruction fetch', 'memory read' or 'stack read' status - as applicable - to the Controller. On application of STSTB, the Controller decodes the status as 'memory read'. The next rising edge of $\Phi 2$ initiates DBIN from the Processor, whereupon the Controller issues a MEMR command to the Bus Control (fig. 6.1.9) and memory, and also sets the Processor Data Bus to the input condition to enable the incoming instruction or data to enter the Processor. The DBIN and MEMR inputs to the Bus Control result in the DIEN (DATA INPUT ENABLE) signal becoming high, setting the Bidirectional Bus Driver to the receive mode and hence establishing communication between the System Data Bus and the Processor Data Bus.

If a hold is requested and a memory read is performed prior to the generation of the hold acknowledge signal HLDA (see Direct Memory Access), MEMR is terminated before the end of DBIN (fig. 6.1.5).

Memory Write (fig. 6.1.1)

When an instruction requires the Microprocessor to write to memory, the first action of the sequence is to place the write address on the Processor Address Bus and to pass 'memory write' or 'stack write' status to the Controller, the latter causing the Controller to decode a 'memory write'. On the rising edge of $\Phi 1$, the Processor outputs WR to the Controller, which responds by generating MEMW to the memory. As all inputs to the Bus Control are normally low during a memory write, the Bidirectional Bus Driver is held in the transmit state (DIEN low), and thus the data output by the Processor during the cycle passes via the Controller Data Bus to the System Data Bus and thence to memory.

IO Read and Write (fig. 6.1.1)

When the Processor wishes to read data from, or write data to, a peripheral device, it places the appropriate addresses on the address bus and transmits 'input read' or 'output write' status to the Controller as required by the operation to be performed. A similar sequence to that involved in reading from, or writing to, memory takes place, but in this instance, one of signals IOR and IOW is also generated by the Controller. The IO signal is gated with the corresponding memory command (MEMR or MEMW) and the address bits ADD14 & 15. If both the latter are true, then the data transfer is initiated by the IORM (INPUT OUTPUT READ MAPPED) or IOWM signal from the Memory Mapped IO Control. In the case of a read, IORM is also used to set the Bidirectional Bus Driver to the receive mode to enable input of data from the System Data Bus to the Processor.

Interrupts (fig. 6.1.9)

Circuit Preparation. In response to an instruction to allow interrupts, the Microprocessor enables the Priority Interrupt Control Unit - by making the INTE (INTERRUPT ENABLE) line high - and performs an IO write at the Control Unit address to enter the current 'mask' information into that unit.

The 'mask' information is contained in bits D0 to D3 of the System Controller Data Bus. Effectively, this information defines which of the possible eight interrupt levels with access to the Control Unit via an INTERRUPT REQUEST line (IRQ0 to IRQ7) is to be allowed to interrupt the Microprocessor. If the SGS (STATUS GROUP SELECT) bit D3 is high, the highest priority interrupt request present is serviced; if SGS is low, a request is serviced only if it is of a higher level of priority than that defined by the complement of the number contained in bits D0 to D2. In the present application, the masking is structured as follows, where 0 is the lowest priority level and 7 the highest.

D3	D2	D1	D0	Requests Serviced
H	X	X	X	All
L	H	H	H	$\overline{\text{IRQ1}} - \overline{\text{IRQ7}}$
L	H	H	L	$\overline{\text{IRQ2}} - \overline{\text{IRQ7}}$
L	H	L	H	$\overline{\text{IRQ3}} - \overline{\text{IRQ7}}$
L	H	L	L	$\overline{\text{IRQ4}} - \overline{\text{IRQ7}}$
L	L	H	H	$\overline{\text{IRQ5}} - \overline{\text{IRQ7}}$
L	L	H	L	$\overline{\text{IRQ6}}, \overline{\text{IRQ7}}$
L	L	L	H	$\overline{\text{IRQ7}}$
L	L	L	L	None

X = irrelevant

The appearance of the port address of the Control Unit on the System Address Bus causes the Address Comparator and Decoder (fig. 6.1.8) to generate an $\overline{\text{S0}}$ (SELECT 0) output. The $\overline{\text{IOWM}}$ pulse that occurs subsequently is gated with $\overline{\text{S0}}$ to produce the ECS (ENABLE CURRENT STATUS) pulse, which loads the mask information into the Control Unit.

Request Handling. At the Priority Interrupt Control Unit, all incoming interrupt requests are first priority-encoded. Providing that no request is currently being serviced, the unit then issues a 3-bit code ($\overline{\text{A0}}$ to $\overline{\text{A2}}$) to the Buffer Register indicating the highest priority level that is active. Within the Control Unit, this code is compared with the previously-loaded mask to ascertain whether requests at that priority level are allowed. If they are, the unit generates an $\overline{\text{INT}}$ (INTERRUPT) signal.

Together with the hard-wired bits at the Buffer Register inputs, $\overline{\text{A0}}$ to $\overline{\text{A2}}$ define the interrupt vector address. This address is strobed into the Buffer Register by $\overline{\text{INT}}$; providing a HOLD has not been requested this event also causes an interrupt request to be input to the Microprocessor.

On completion of the current instruction the Microprocessor acknowledges the request by outputting $\overline{\text{INTA}}$ low. This enables the Buffer Register outputs onto the Controller Data Bus and the interrupt vector address is thus passed to the Microprocessor, which then commences operations at the appropriate Restart ($\overline{\text{RST0-7}}$), specified as below. The return to the main program is controlled by software.

The least significant output bit of the PA Buffer Register is combined with the 8-bit output of the CB Buffer Register and the 9-bits so obtained compared with the 9-bit refresh address (RFA0 to RFA8) to provide CB (Cursor Bit) with a unique address (each display address is one character slot on the screen).

It should be noted that the l.s.b. of the PA Buffer Register output becomes the m.s.b. of the cursor bit address, thereby defining which buffer register provides the character position of the cursor within that half page. Complete cursor addressing must therefore be performed in two stages. Data is latched into the buffer registers from the data bus by a combination of CW (Cursor Write) and either $\overline{S1}$ or $\overline{S2}$. Signal CW is the inverse form of $\overline{IOWM}$ and it is via the IO logic and the instruction that cursor addressing is implemented.

Address Multiplexing. Address outputs from the board circuits are placed on the System Address Bus via a pair of 2 line-to-1 line multiplexers which operate under the control of the D.M.A. acknowledge signals. In the present application of the board, $\overline{DACK1}$ and $\overline{DACK2}$ are permanently high (see Direct Memory Access) and hence the multiplexer outputs are permanently enabled. During normal working, therefore, the states of $\overline{ADD0}$ to $\overline{ADD15}$ are defined by the contents of the Processor Address Bus A0 to A15. However, when, during a refresh cycle, $\overline{RFACK}$ goes low to acknowledge the refresh request, the multiplexers replace the normal address bits with refresh address bits RFA0 to RFA9, page address bits PA9 to PA15.

register. One clock period after HLDA, therefore, T4 becomes high for one period, enabling the RFACK (REFRESH ACKNOWLEDGE) output for approximately half a period, at the end of which period the Ack bistable is reset. On the next rising edge of $\Phi 2$ (TTL), QC becomes high and so the Hold Request latch is cleared via the And-Or-Invert element, removing the HOLD input to the Processor. Approximately one $\Phi 2$ period later, the Processor makes HLDA low. As RFACK has already caused RFREQ to be reset high, the circuit is thus returned to the quiescent condition.

Typical D.M.A. timing is shown in fig. 6.1.7.

Bus Control and Addressing. In order to perform a D.M.A., the System Address and Data Busses must be handed over to the initiator of the request and an address of the correct value must be generated.

The D.M.A. address is generated by the synchronous D.M.A. Address counter; this produces 512 addresses that are incremented by DMA0 applied to the clock input of the element. The Microprocessor 'floats' its address lines during HLDA and RFACK multiplexes the REFRESH ADDRESS onto the System Address Bus (fig. 6.1.8).

In the case of the System Data Bus, control is handled by the System Controller and Bus Driver. Application of HLDA to the Controller is followed after some 125 ns by the BUSEN input to that element becoming high, thus isolating the Processor Data Bus from the System Data Bus.

I.C.E. Working. When the F.R.A. is in the I.C.E. mode and 'not ready' during a D.M.A., the Processor cannot produce HLDA. The signal must therefore be simulated.

The simulation is enabled by setting link LK1 to position I. As LSL is high during the D.M.A. this results in a DELAYED HOLD signal being or'ed onto the HLDA line (fig. 6.1.1).

Via the And-Or-Invert element, LSL is also used to clear the Hold Request latch after 32 D.M.A. cycles, thus ensuring that the circuit is correctly reset.

Address Selection and Multiplexing (fig. 6.1.8)

Address Selection. At the input of the Address Selection and Multiplexing circuit, address bits ADD3 to ADD7 are compared with the address set in at the Processor Interrupt Address Select switch array. The resultant of this operation and the least significant address bits ADD0 to ADD2 are then decoded to provide SELECT signals S0, S1 and S2 (interrupt address, page address and cursor bit address, respectively).

Signal S0 is gated with the inverse form of IOWM to generate the ECS signal to the Priority Interrupt Control Unit. Signals S1 and S2 are used to enable the PA and CB Buffer Registers.

The PA Buffer Register provides the PAGE ADDRESS bits PA9 to PA15, for multiplexing onto the System Address Bus as the page address to memory during a memory refresh cycle (any one of thirty-one pages may be selected).

The least significant output bit of the PA Buffer Register is combined with the 8-bit output of the CB Buffer Register and the 9-bits so obtained compared with the 9-bit refresh address (RFA0 to RFA8) to provide CB (Cursor Bit) with a unique address (each display address is one character slot on the screen).

It should be noted that the l.s.b. of the PA Buffer Register output becomes the m.s.b. of the cursor bit address, thereby defining which buffer register provides the character position of the cursor within that half page. Complete cursor addressing must therefore be performed in two stages. Data is latched into the buffer registers from the data bus by a combination of CW (Cursor Write) and either $\overline{S1}$ or $\overline{S2}$. Signal CW is the inverse form of $\overline{IOWM}$ and it is via the IO logic and the instruction that cursor addressing is implemented.

Address Multiplexing. Address outputs from the board circuits are placed on the System Address Bus via a pair of 2 line-to-1 line multiplexers which operate under the control of the D.M.A. acknowledge signals. In the present application of the board, $\overline{DACK1}$ and $\overline{DACK2}$ are permanently high (see Direct Memory Access) and hence the multiplexer outputs are permanently enabled. During normal working, therefore, the states of $\overline{ADD0}$ to $\overline{ADD15}$ are defined by the contents of the Processor Address Bus A0 to A15. However, when, during a refresh cycle, $\overline{RFACK}$ goes low to acknowledge the refresh request, the multiplexers replace the normal address bits with refresh address bits RFA0 to RFA9, page address bits PA9 to PA15.

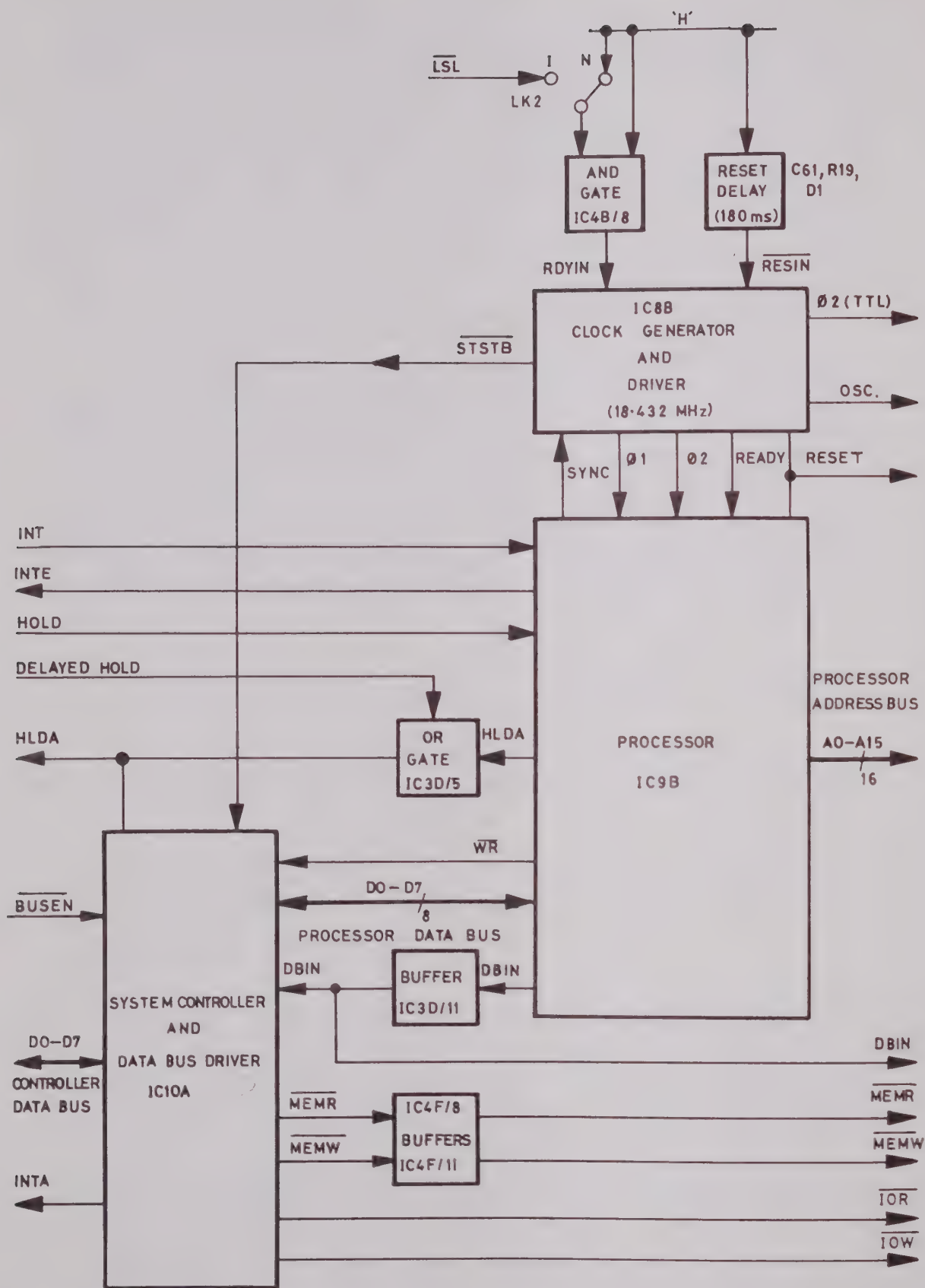


FIG.6-1-1 MICROPROCESSOR

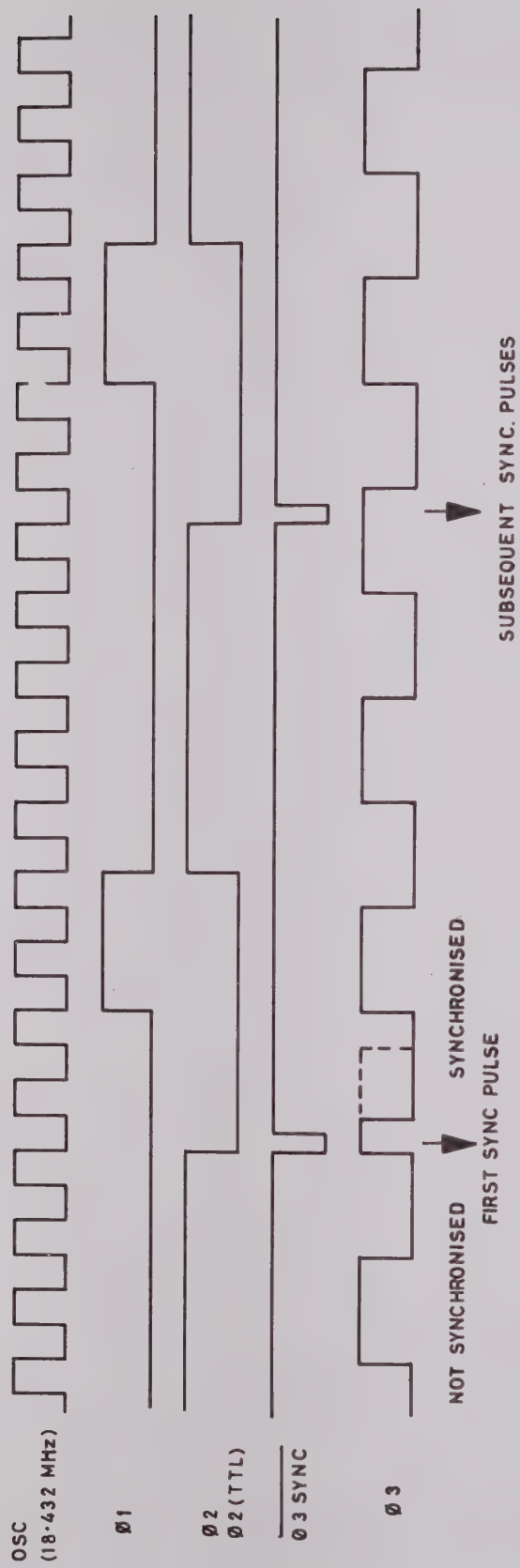


FIG 6.1.2 CLOCK GENERATION AND SYNCHRONIZATION

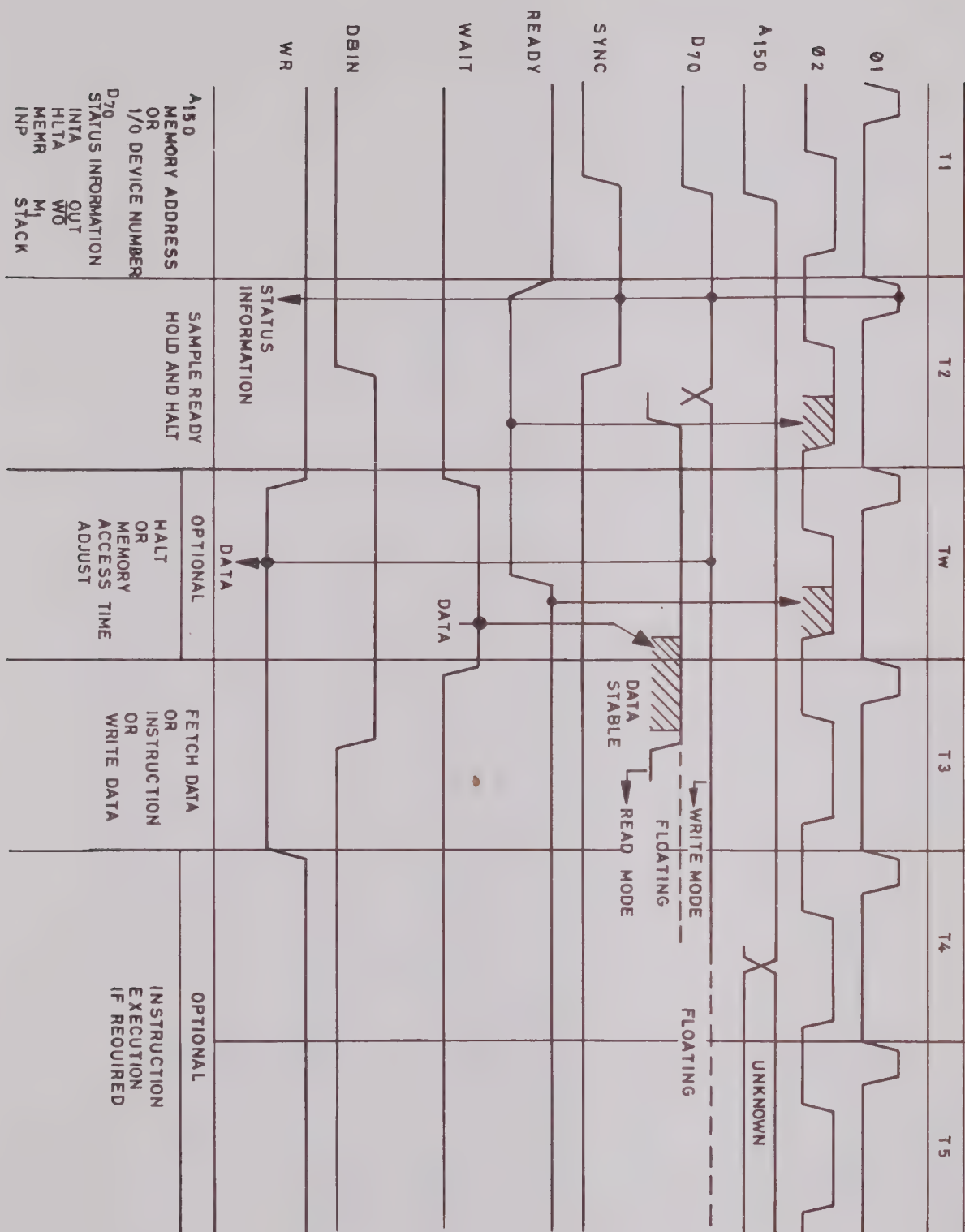


FIG. 6.1.3 BASIC INSTRUCTION CYCLE TIMING

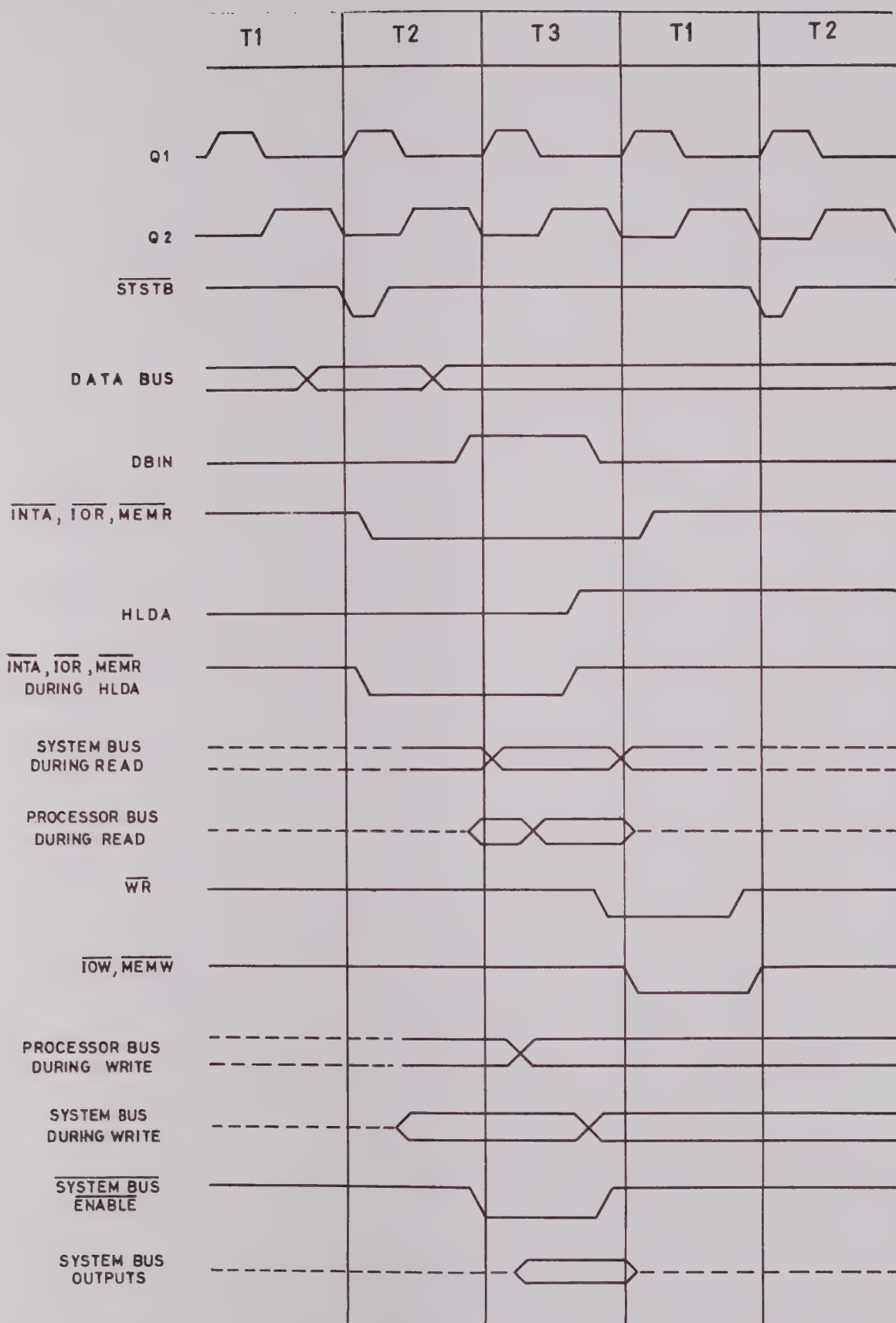


FIG 6.1.4 TYPICAL CONTROLLER TIMING

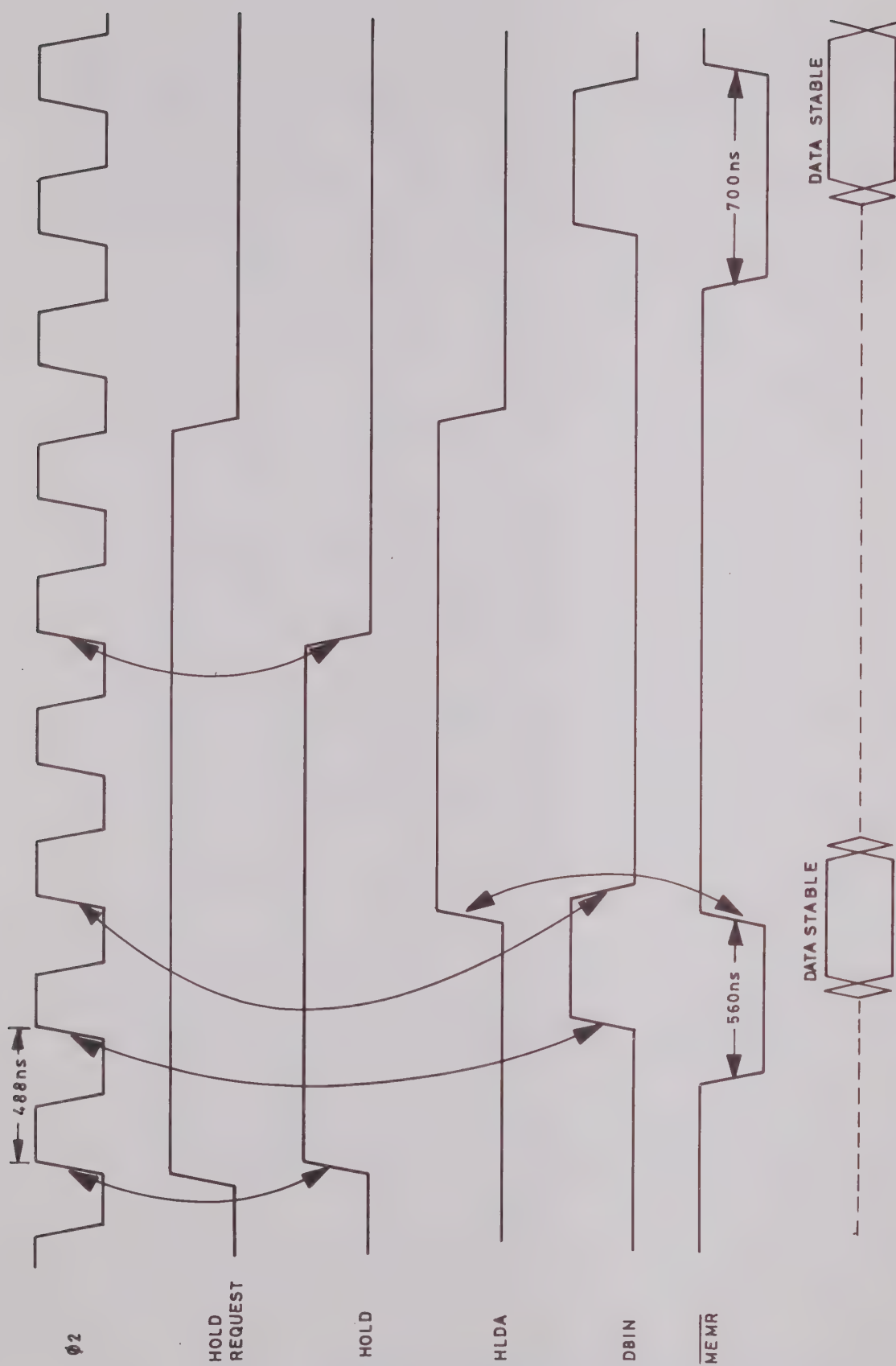
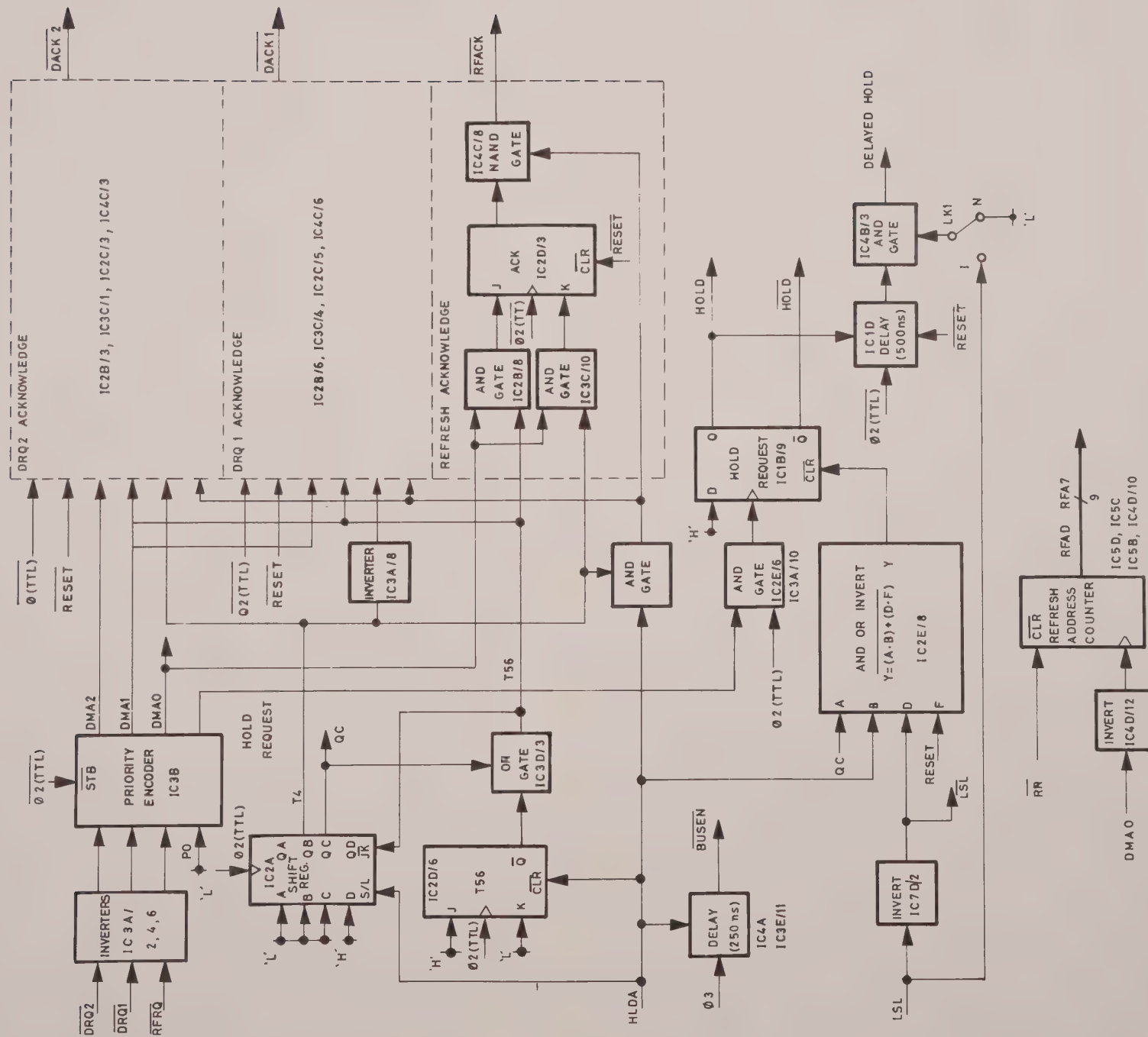


FIG. 6.1.5 TYPICAL HOLD TIMING



DMA LOGIC FIG. 6-1-6

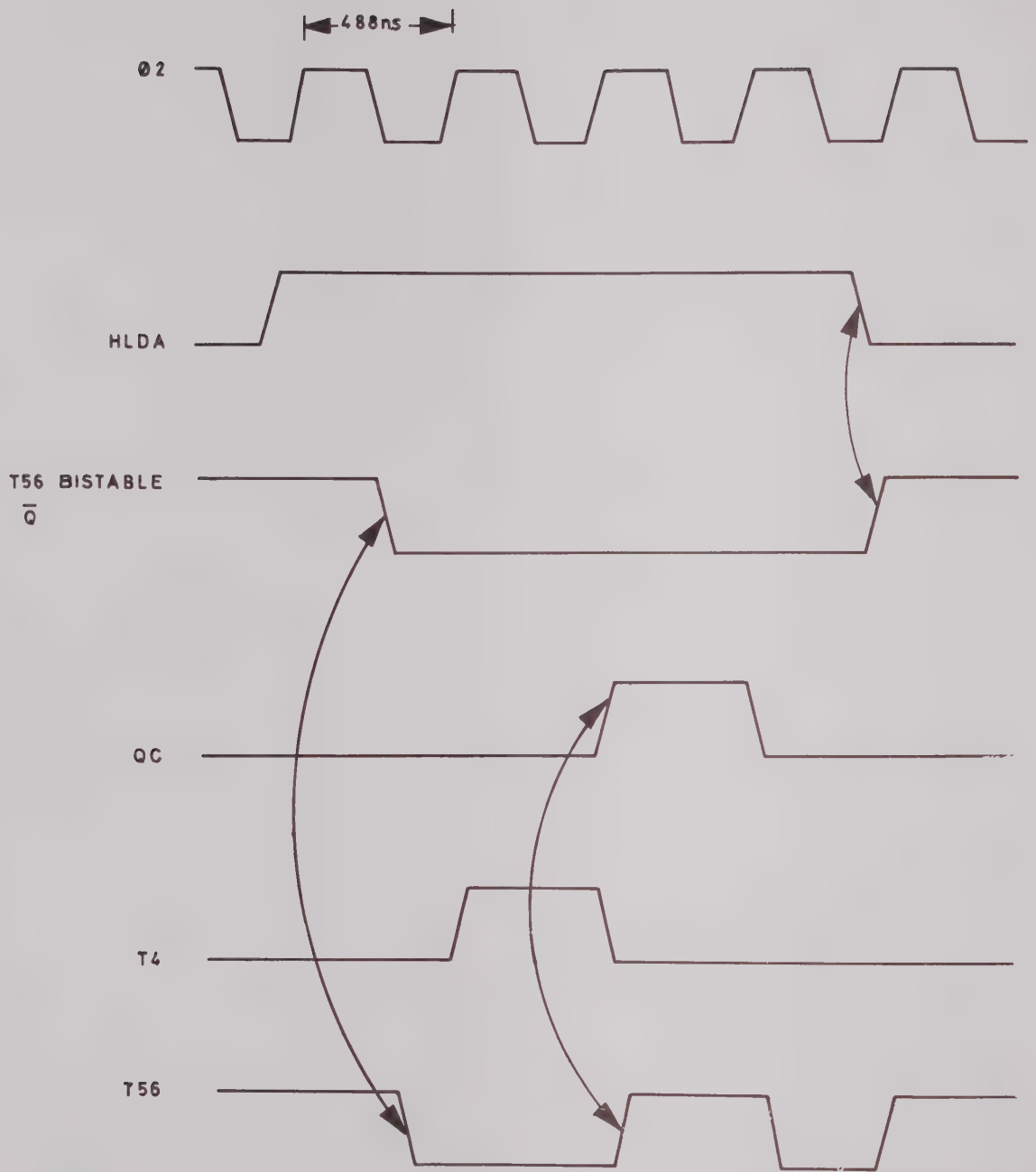
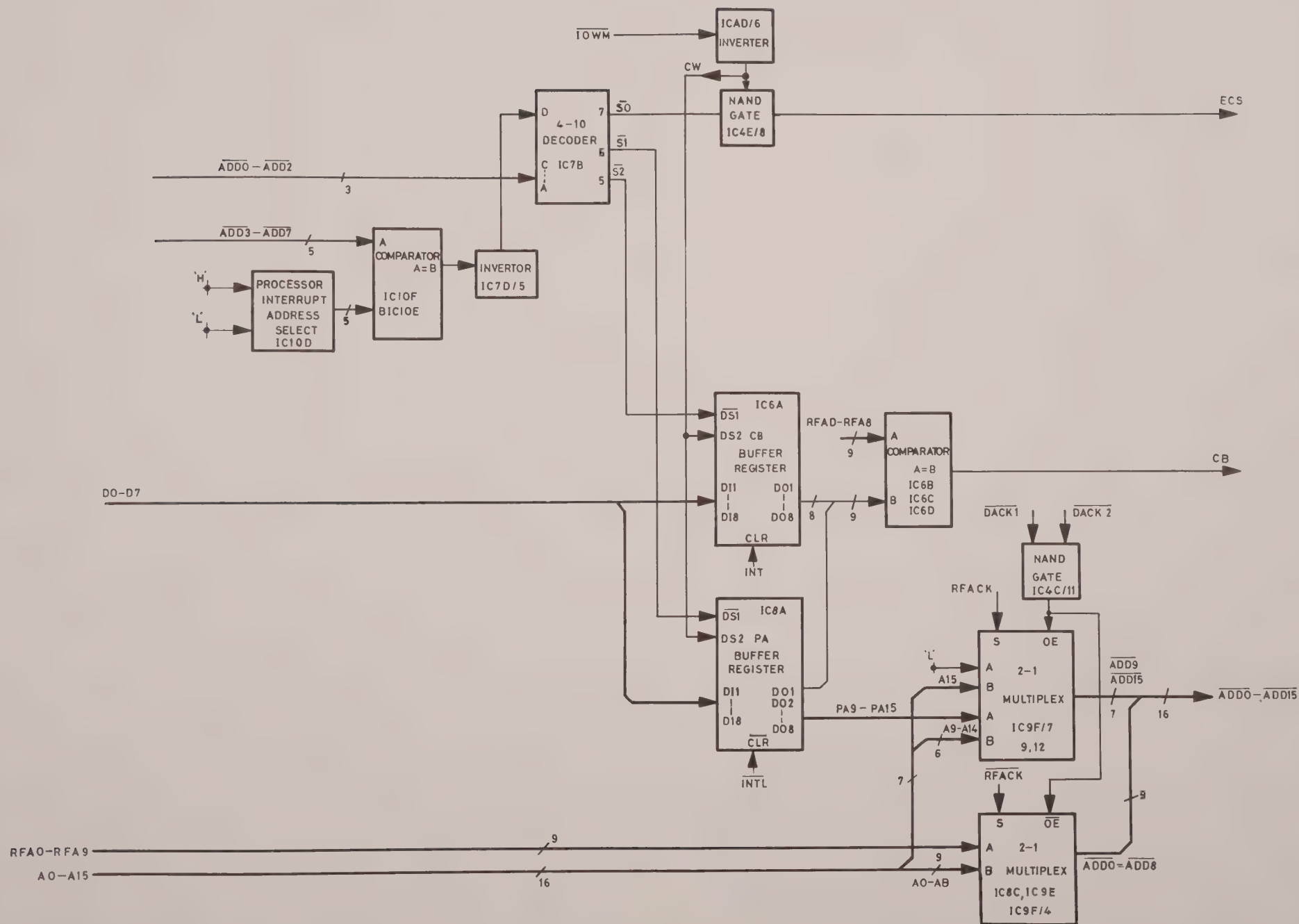
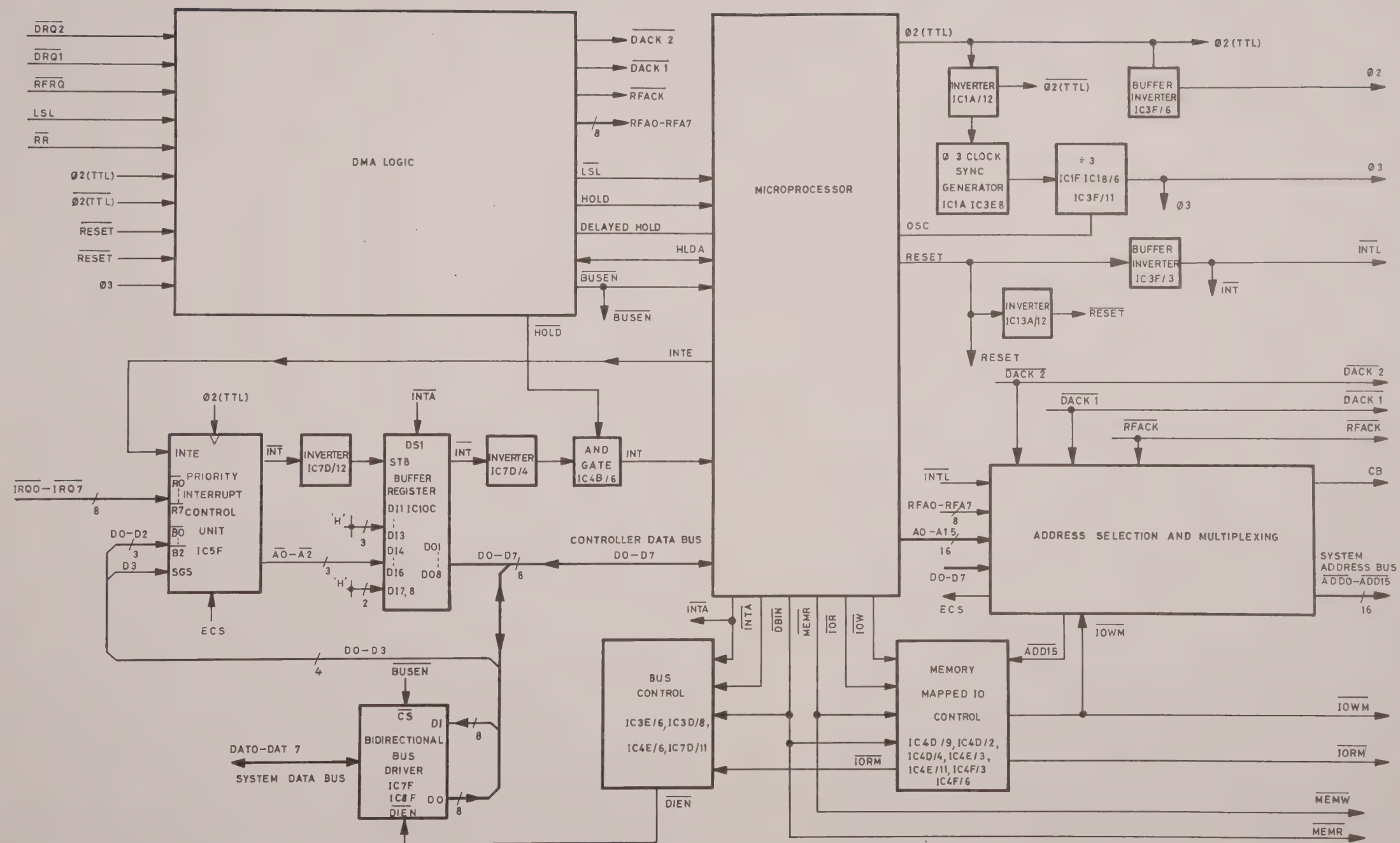


FIG. 6-1-7 TYPICAL DMA TIMING



ADDRESS SELECTION AND MULTIPLEXING FIG. 6.1.8



PROCESSOR AND CURSOR CONTROL BOARD

MEMORY BOARD 1

Introduction

The Memory Board provides storage for 24,576 words of eight bits length. 16,384 words of storage are in the form of programmable read only memory (PROM) which is used to hold the F.R.A. control operations program. The remaining 8,192-word capacity is in the form of random access memory (RAM) which is used as a scratchpad for calculations, stacks, results and display. The store addresses run from 0000 to 3FFF Hexadecimal for the program store and from 4000 to 5FFF for the scratchpad store.

A functional block diagram of the board is shown in fig. 6.2.3.

OPERATION

The Timing and Control Logic is complicated by the RAM store requiring its address to be presented in two cycles as row and column addresses. The PROM store, however, uses a direct address. The stores are also organised in different manners. The PROM store comprises eight, 2K, 8-bit word areas, each of which is held on one integrated circuit chip. The RAM store is organised into two areas of 4K, 8-bit words, each area comprising eight, 4K x 1-bit store chips.

Power-On Reset

When the F.R.A. is switched on, the Processor and Cursor Control Board sends an INITIALISE (INTL) pulse which, on going low, clears the Input and Output Buffers.

Read (PROM Memory)

When a store read is required, the address of the store location is placed on the Address Highway (ADD0 to ADD15) and, approximately 250 ns later, the Processor and Cursor Control Board generates the MEMORY READ signal MEMR. ADD14 is low for all PROM addresses, which together with READ and ADD11, 12 and 13 enables the Program Store Area Decoder to generate one of the PCS0 to PCS7 waveforms. The 11 l.s.b. of the address together with one of the PCS0 to PCS7 waveforms locates the data which is read into the Output Buffer.

READ is initiated by MEMR but is terminated by the Data Output latch (IC6C/9), which itself is cleared by delayed MEMR extended by a $\Phi 3$ period. The Data Output latch gates the data from the Output Buffer onto the System Data Bus (DAT0 to DAT7). The read timing is shown in fig. 6.2.1.

Read (RAM Memory)

The MK 4027P3 RAMs are dynamic in operation, i.e. they require to be refreshed by reading at least every 2 ms. As it is also necessary for the display to receive data within this period, this operation and the refresh cycle have been combined by using the signal RFACK (REFRESH ACKNOWLEDGE) to initiate the sequence. As far as the RAM storage is

concerned, $\overline{\text{MEMR}}$ and $\overline{\text{RFACK}}$ have the same effect. Therefore only the Read cycle with $\overline{\text{MEMR}}$ is described.

When a Read cycle is required, the address of the store location is placed on the Address Highway (ADD0 to ADD15) and, approximately 250 ns later, the Processor and Cursor Control Board generates the memory read signal ($\overline{\text{MEMR}}$). ADD14 is high for all RAM addresses and therefore the Program Store Area Decoder is inhibited but the Scratchpad Area Decoder decodes which half of the Scratchpad is required. COLUMN SELECT is low, thus the Column/Row Address Selector selects the row address from ADD0 to ADD5 and CAS ($\text{COLUMN ADDRESS STROBE}$) is high. $\overline{\text{MEMR}}$ after passing through IC9C/2, 9C/12 and 7C/8 sets the Data Output latch (IC6C/9), which generates O/P BUFFER ENABLE. This, together with ADD15 being low (ADD15 is only high for input/output peripheral operations), opens the Output Buffer onto the System Data Bus. Shortly after the setting of the Data Output latch, RAS ($\text{ROW ADDRESS STROBE}$) goes low to gate the row address into the required RAM chips.

The output of gate IC5C/3 is also fed through a delay (IC5C/6, 5C/8, 4C/4 and 4C/1) to the Column latch (IC6C/5). (The delay, which relies on the propagation delays of gates, ensures that the rising edge input to the Column latch does not coincide with, or shortly precede, a rising edge of the $\Phi 3$ clock). This delay, plus the delay of nearly one $\Phi 3$ clock period in setting the Column latch and the succeeding delay (IC7C/3), allows the row address to be presented to the RAM for the required recognition period before the selection of the column address. COLUMN SELECT going high causes the Column/Row Address Selector to select ADD6 to ADD11 (the column address). The Column/Row Address Selector logic contains a gate (IC7C/11) the propagation delay of which allows for the set-up time of the column address before the negative edge of $\overline{\text{CAS}}$ strobes the address into the RAM chip. The data appears as DATA OUT 0 to 7 approximately 135 ns after the generation of $\overline{\text{CAS}}$.

The Read cycle timing is illustrated in fig. 6.2.2.

Write (RAM Memory)

The Timing and Control Logic treats the Write command in a similar manner to the Read command. One additional waveform, WRITE , is generated but the Data Output latch (IC6C/9) is not set for this operation. The data to be written to the store is presented on the System Data Bus in synchronism with $\overline{\text{MEMW}}$ (MEMORY WRITE). WRITE is generated by Anding RAS with a delayed $\overline{\text{MEMW}}$ (IC2C/1, IC/2). The data is written into the RAM on the negative edge of CAS .

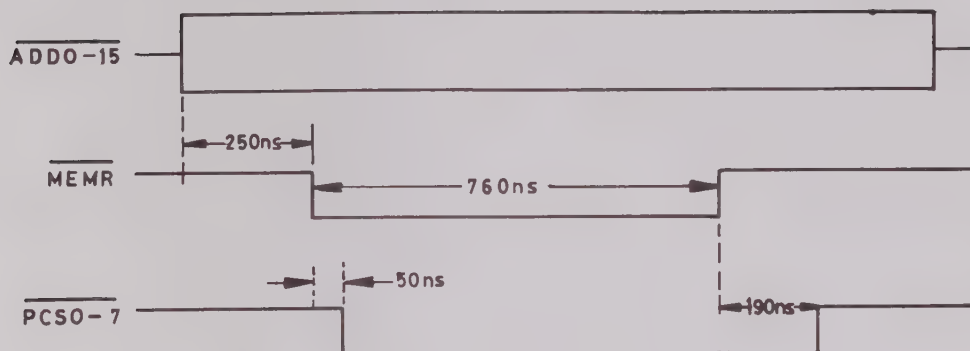


FIG. 6-2-1 PROM READ TIMING

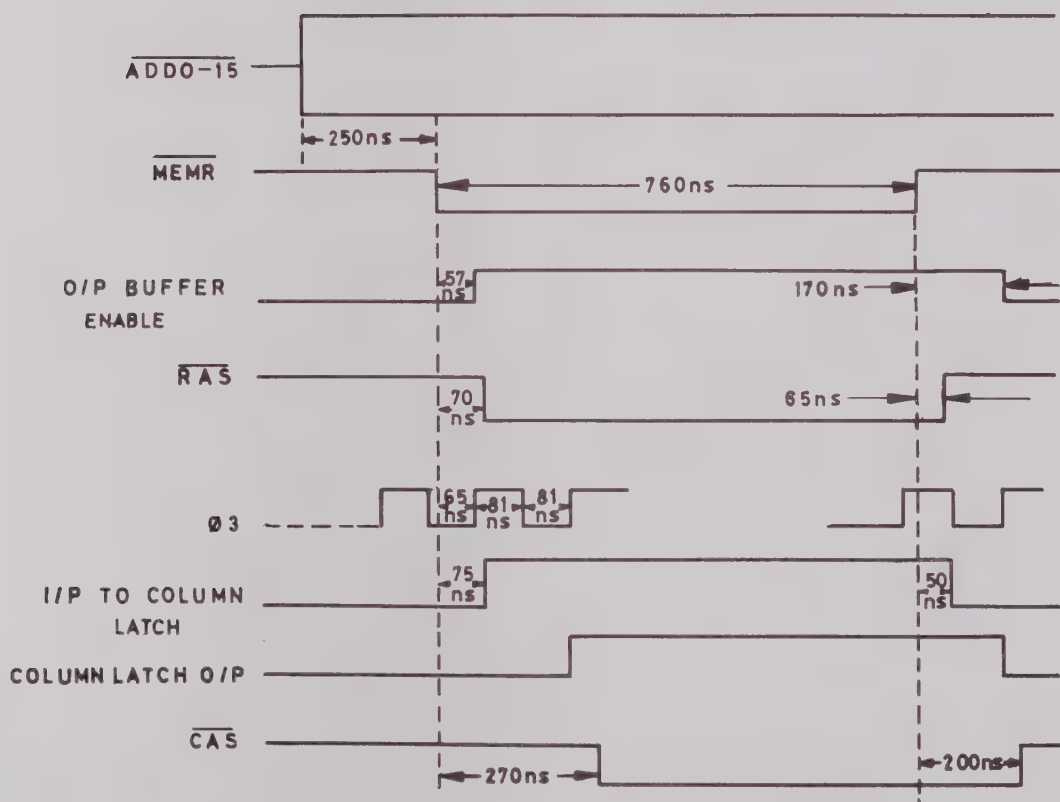
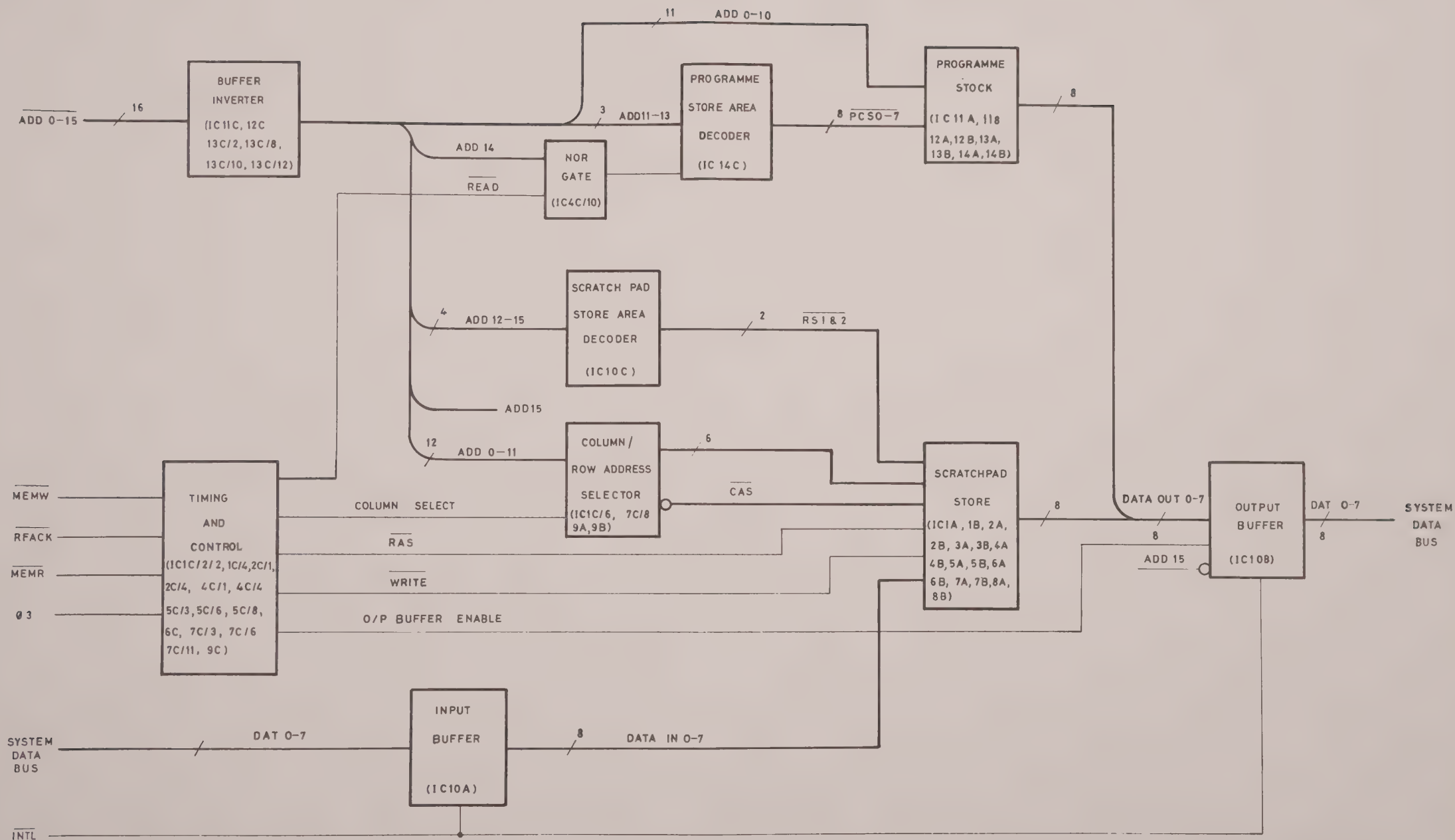
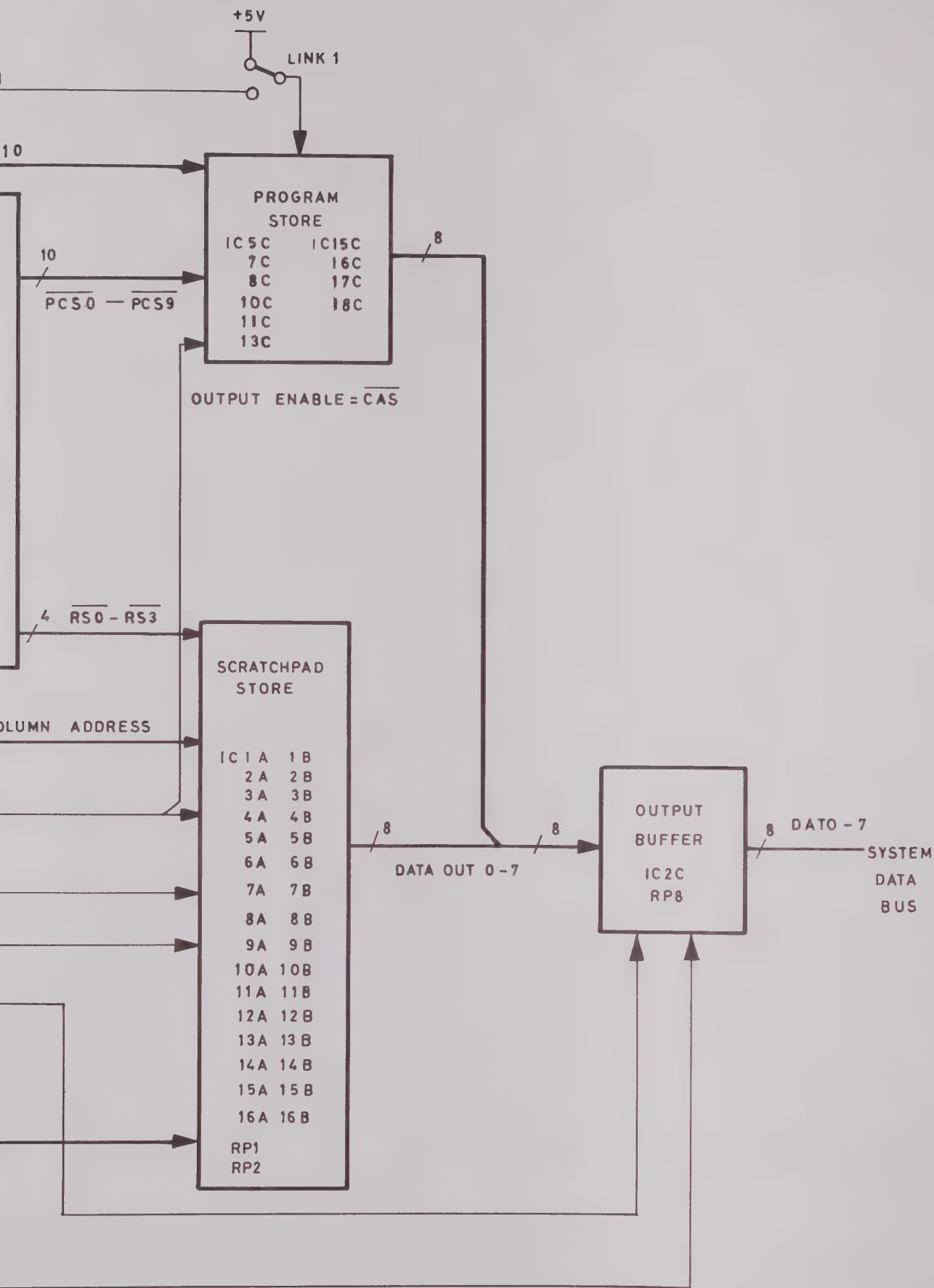


FIG. 6-2-2 RAM READ TIMING



MEMORY BOARD FIG. 6-2-3



MEMORY 2 BOARD FIG. 6.2.4.

MEMORY BOARD 2 (E90917, Issue 2)

Introduction

The memory 2 board provides storage for 49,152 words of eight bits length. Up to 32,768 words of storage are in the form of programmable read-only memory (PROM) which is used to hold the control operations program. The remaining 16,384 word capacity is in the form of random access memory (RAM) which is used for calculations, stacks, results and display. The program store addresses run from 0000 to 7FFF hexadecimal and the RAM store from 8000 to BFFF hexadecimal.

Provision has been made in the design for future expansion of the program store.

A functional block diagram of the memory 2 board is shown in fig 6.2.4.

OPERATION

The PROM store is organised in blocks of 2048 words of eight bits, each block being held on one integrated circuit; the number of integrated circuits required depending on the version of software installed.

The RAM store is arranged as four areas of 4096, 8-bit words, each area being held on eight 4096 x 1-bit chips.

Power-On Reset

When the SE 2450 is switched on, the processor and cursor control board sends an INITIALIZE (INTL) pulse which, on going low, clears the input and output buffers.

Store Addressing

The RAM store requires its address to be presented in two cycles as row and column addresses. The PROM store uses direct addressing. These two different modes of addressing are dealt with by feeding the system address lines ADD0 to ADD11 directly to the PROM area, and multiplexing them into two groups of six in the column/row address selector before applying them to the RAM area.

The two stores are located in the system memory map by an address decoder, which monitors the state of the most significant five address lines ADD12 to ADD15. The decoder is a pre-programmed ROM (IC13D and IC15D) arranged so that the sixteen data output lines generate the ten PROM enable signals PCS0 to PCS9, the four RAM enable lines RS0 to RS3 and the Memory Enable (MEMEN) signal. Figure 6.2.5 shows the bit pattern in the ROM.

Read (PROM Memory)

When a store read is required, the address of the store location is placed on the Address Highway (ADD0 to ADD15) and, approximately 250 ns later, the Processor and Cursor Control Board generates the MEMORY READ signal MEMR. ADD15 is low for all PROM addresses, which together with READ and ADD12 to ADD14 enables the Store Address Decoder to generate one of the PCS0 to PCS9 waveforms. The 11 l.s.bits of the address together with one of the PCS0 to PCS9 waveforms locates the data which is read into the output buffer.

READ is initiated by MEMR but is terminated by the data output latch (IC7D/9), which itself is cleared by delayed MEMR extended by a $\phi 3$ period. The data output latch gates the data from the output buffer onto the system data bus (DAT0 to DAT7). The read timing is shown in fig 6.2.6.

Read (RAM Memory)

The MK 4027P3 RAMs are dynamic in operation, i.e. they require to be refreshed by reading at least every 2 ms. As it is also necessary for the display to receive data within this period, this operation and the refresh cycle have been combined by using the signal RFACK (REFRESH ACKNOWLEDGE) to initiate the sequence. As far as the RAM storage is concerned, MEMR or RFACK have the same effect. Therefore only the read cycle with MEMR is described.

When a read cycle is required, the address of the store location is placed on the address highway (ADD0 to ADD15) and, approximately 250 ns later, the processor and cursor control board generates the memory read signal (MEMR).

COLUMN SELECT (IC7D/5) after being delayed by IC9D/3 is applied to the ROW/COLUMN address selector IC17A and 17B.

When COLUMN SELECT is low, the row address is selected from ADD0 to ADD5, and CAS (COLUMN ADDRESS STROBE) is high. MEMR after passing through delays IC10D/2, IC10D/12 and OR gate IC6D/11, sets the data output latch IC7D/9 provided that MEMEN is high at IC4D/13. O/P BUFFER ENABLE from IC7D/9 opens the output buffer onto the system data bus.

Shortly after the setting of the data output latch, RAS (ROW ADDRESS STROBE) goes low to gate the row address into the required RAM chips.

The output of gate IC6D/3 is also fed through a delay (IC6D/6), IC6D/8, IC4D/3 and IC4D/6 to the column latch (IC7D/5). (The delay which relies on the propagation delays of gates, ensures that the rising edge input to the column latch does not coincide with, or shortly precede, a rising edge of the $\phi 3$ clock). This delay, plus the delay of nearly one $\phi 3$ clock period in setting the column latch and the succeeding delay (IC9D/3), allows the row address to be presented to the RAM for the required recognition period before the selection of the column address. COLUMN SELECT going high causes the column/row address selector to select ADD6 to ADD11 (the column address). The column/row address selector logic contains gates IC9D/11, IC1D/4, the propagation delay

ROM REF.	FUNCTION	PROGRAM STORE ↔ 20K PROM										SCRATCHED STORE ↔ 16K RAM																					
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
ADD	E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	C	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	
	B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	
	A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
IC15D	DO	0																															
	DI		0																														
	D2			0																													
	D3				0																												
	D4					0																											
	D5						0																										
	D6							0																									
	D7								0																								
	IC13D	DO										0																					
		D1											0																				
		D2												0																			
		D3													0																		
		D4														0																	
D5															0																		
D6																0																	
D7																	0																
D0	PCS0																																
D1	PCS1																																
D2	PCS2																																
D3	PCS3																																
D4	PCS4																																
D5	PCS5																																
D6	PCS6																																
D7	PCS7																																
D0	PCS8																																
D1	PCS9																																
D2	MEMEN																																
D3																																	
D4	RS0																																
D5	RS1																																
D6	RS2																																
D7	RS3																																

NOTE: ALL UNMARKED BITS ARE '1'S

FIG 6.2.5. STORE ADDRESS DECODER ROM

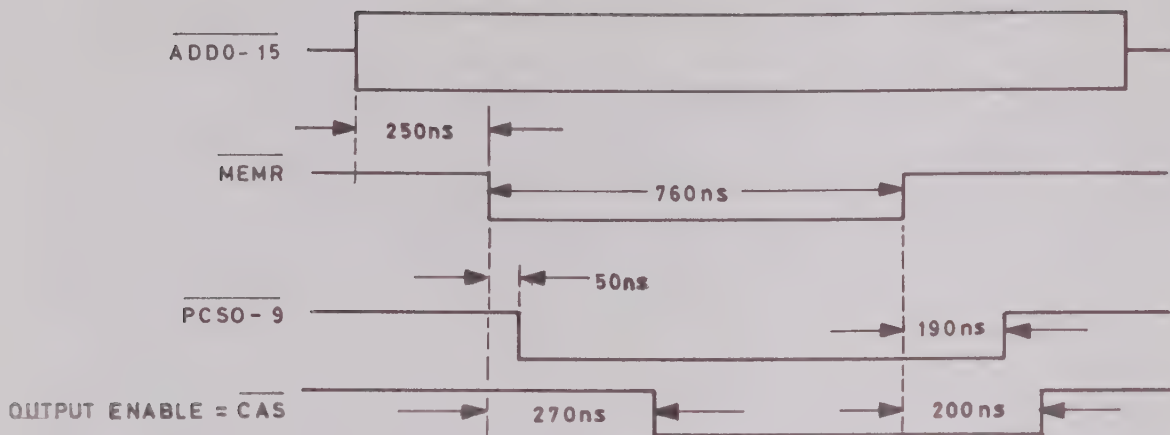


FIG. 6.2.6. PROM READ TIMING (MEM 2)

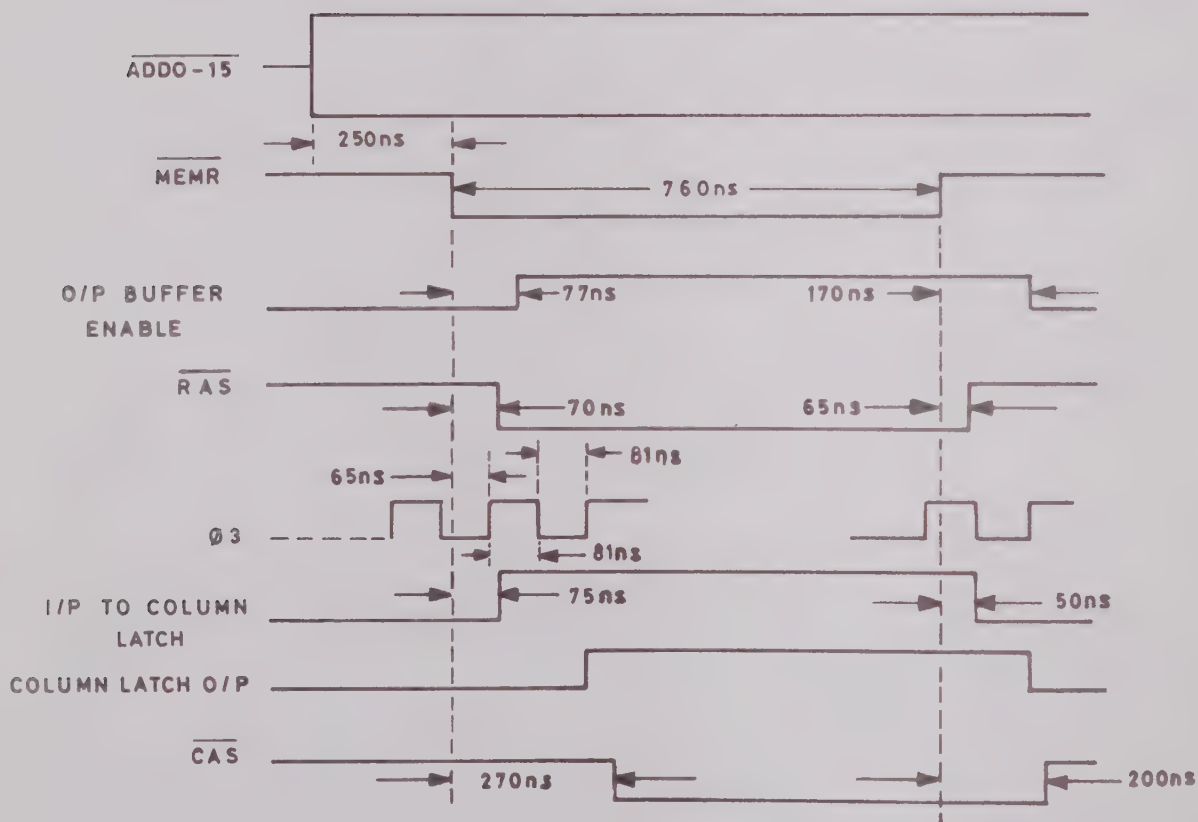


FIG. 6.2.7. RAM READ TIMING (MEM 2)

of which allows for the set-up time of the column address before the negative edge of $\overline{\text{CAS}}$ strobes the address into the RAM chips. The data appears as DATA OUT 0 to 7 approximately 135 ns after the generation of $\overline{\text{CAS}}$.

The read cycle timing is illustrated in fig 6.2.7.

Write (RAM Memory)

The timing and control logic treats the Write command in a similar manner to the Read command. One additional waveform, $\overline{\text{WRITE}}$, is generated but the data output latch (IC7D/9) is not set for this operation. The data to be written to the store is presented on the system data bus in synchronism with $\overline{\text{MEMW}}$ (MEMORY WRITE). $\overline{\text{WRITE}}$ is generated by Anding $\overline{\text{RAS}}$ with a delay $\overline{\text{MEMW}}$ (IC3D/1, IC1D/2). The data is written into the RAM on the negative edge of $\overline{\text{CAS}}$.

GENERATOR CONTROL BOARD

CHAPTER 6.3

Introduction

The Generator Control Board:

- (a) Provides an interface for the exchange of data and control signals between the Generator and Microprocessor functions.
- (b) Generates two, TTL-compatible, output signals - one at a known fundamental frequency and one at a known harmonic of that fundamental - which are multiples of an accurate, internally-generated, reference frequency.

A functional block diagram of the board is shown in fig. 6.3.2.

OPERATION

Interfacing

The Vector Address Comparator constantly monitors the System Address Bus bits ADD3 to ADD7 and the IOWM (INPUT OUTPUT WRITE MAPPED) control line. When the value of the address bits equals the value set in at the Address Selector switch array - i.e. when the address on the bus is within the range of vector and port addresses allocated to the generator function (40 Hex. to 47 Hex.) - concurrent with IOWM being low, the comparator applies a low to the m.s. input of the Port Address Decoder.

The three l.s. inputs to the Port Address Decoder are provided by the three l.s.b. of the System Address Bus (ADD0 to ADD2). With the m.s. input high, the decoder which result from this arrangement are outside the range indicated by decoder outputs SG0 to SG7 (SELECT GENERATOR 0 to 7) and these signals thus remain low. The change of state of the m.s. input to low rectifies this 'out of range' condition and so the SELECT GENERATOR signal defined by ADD0 to ADD2 becomes low, selecting the corresponding interface register (port) as the device to which information will be written during subsequent operations. Eight interface registers are provided in the generator function; details of the registers are given in table 6.3.1 at the end of this chapter.

The interface between the System Data Bus and the Generator Data Bus is provided by an 8-bit buffer register. This register is permanently enabled into the 'transparent' mode and hence the Generator Data Bus always follows the System Data Bus.

Generation of Reference Frequency

In the present application, a reference frequency of 1024 Hz is used. This is obtained by dividing by 10,000 the output of a 10.24 MHz, crystal-controlled oscillator.

Generation of Fundamental and Harmonic Signals

The circuit arrangement utilised for the generation of the FUNDAMENTAL (FNDL) and HARMONIC (HMNC) signal outputs is shown in simplified form

in the block diagram of fig. 6.3.1. The operation of the various components of this arrangement are described in the subsections which follow.

Phase Locked Loop

Operation. In the Phase Locked Loop (P.L.L.), the output of the Phase Detector - i.e. the voltage analogue of the phase difference between the Reference Frequency signal and the pulse train output of the Programmable Counter - is connected to the frequency control input of each of a pair of Voltage Controlled Oscillators (V.C.O.) via the Low-pass Filter and the Amplifier.

As described later, only one of the V.C.O. is enabled at any one time. Following buffering and inversion by the associated Nand-gate, the output of the selected V.C.O. is passed to the loop output and is also used to clock the Programmable Counter.

At the start of the P.L.L. cycle of operation, the Programmable Counter is loaded with a 14-bit binary word representing the complement of the current frequency mantissa and held in the Frequency Mantissa interface registers. The clock pulses cause the Counter to count up from the loaded value, through maximum to zero (i.e. to effectively count down from the true value to zero). On returning to zero, the Counter outputs a 500 μ s logic low pulse, which is used for the phase detection operation and also causes the contents of the interface registers to be loaded into the Counter again. The cycle then repeats, using this value of mantissa.

V.C.O. Selection. The P.L.L. is required to have an output frequency range of from 5.12 MHz to 10.24 MHz. Because of the limited capture range of a V.C.O., it is necessary to divide the output frequency range into upper and lower bands of 5.12 MHz to 7.68 MHz and 7.68 MHz to 10.24 MHz respectively, and to provide a V.C.O. for each band. Which frequency band is demanded at any time is indicated by the states of the m.s.b. and 3rd m.s.b. of the frequency mantissa word, both of which are high when the loop output frequency is to be within the lower band; Nand-gate IC8A/6 constantly monitors for this condition and, in conjunction with Inverter IC10/12, generates a signal which enables the V.C.O. dedicated to the wanted frequency band and disables that dedicated to the unwanted frequency band.

Frequency Exponent Multiplexer

At the Frequency Exponent Multiplexer, the P.L.L. output frequency is divided down by the 28-bit Binary Divider to obtain twenty-eight submultiple powers of two, the lowest frequency thus made available being $\frac{5.12}{2^{28}}$ MHz (≈ 0.02 Hz).

The submultiples are input to the 32-bit Multiplexer, the remaining four inputs to which are provided by the P.L.L. output signal and three hard-wired bits. The order of (binary) magnitude of the required frequency is defined by the 5-bit output of the Frequency Exponent interface register, which control the multiplexer data source selection. Thus the multiplexer output signal is at the selected harmonic frequency numerically multiplied by 1024_{10} .

After buffering, the output signal is made available at the board output (HMNC) for connection to the Correlator Control Board. Also, it is connected directly to the input of the Fundamental Generator.

Fundamental Generator

The fundamental frequency is obtained by dividing the output of the Frequency Exponent Multiplexer by the number between 1 and 15, the complement of which is currently being output by the Harmonic interface register.

Two stages of division are provided, a $\div 15$ Programmable Counter and a $\div 2$ gating arrangement. The Counter is loaded with the contents of the interface register and clocked by the harmonic signal. Thus as in the P.L.L., the element effectively counts down to zero from the true exponent. Each time the count reaches zero, an output pulse is generated, this passing to the $\div 2$ Gating and also being used to reload the Counter.

The Counter on its own can only provide division within the range $\div 2$ to $\div 15$, and the $\div 2$ Gating is provided to enable the board to cater for the $\div 1$ requirement, as indicated by the m.s. bit of the Harmonic word. Thus if the bit is low, indicating a harmonic between 2 and 15, then the counter output provides the generator output signal; if the bit is high, indicating the 1st harmonic, then the counter output is blocked and the output of the Frequency Exponent Multiplexer is gated through to the generator output. In either case, the generator output signal is at the selected fundamental frequency numerically multiplied by 1024_{10} .

The generator output is passed directly to the board output (FNDL) for connection to the Generator Digital-to-Analogue Board.

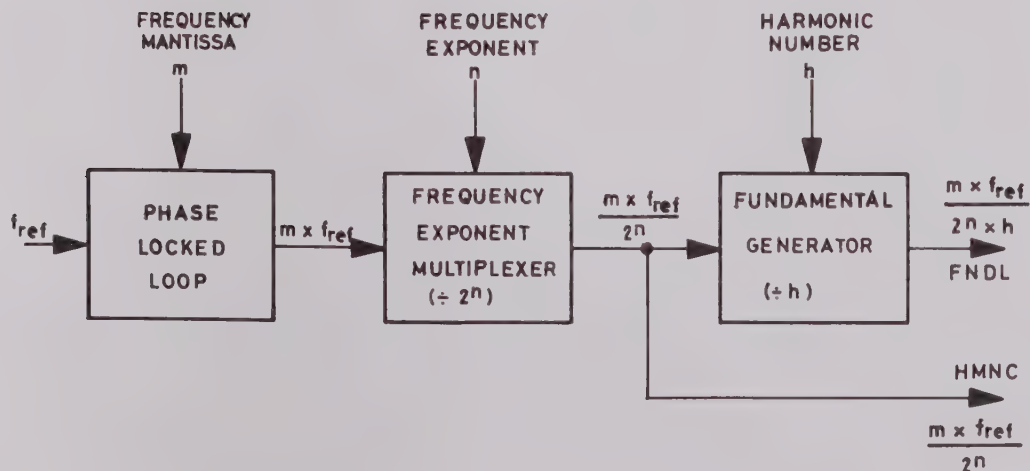
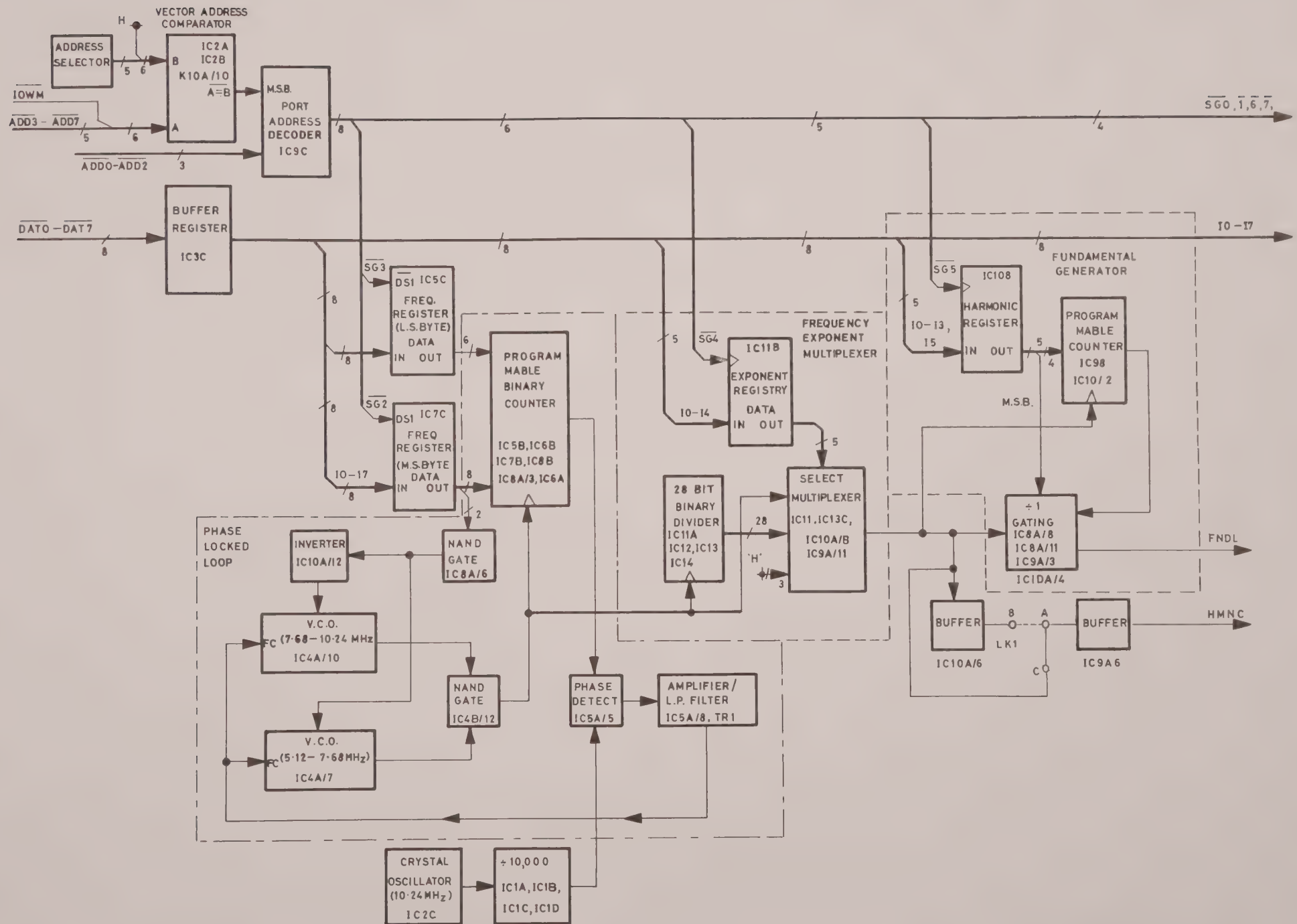


FIG 6. 3. 1. FUNDAMENTAL AND HARMONIC SIGNAL GENERATION

TABLE 6-3-1 INTERFACE REGISTERS DETAILS

ADDRESS (HEX)	40	41	42	43	44	45	46	47
SELECT GENERATOR	SG0	SG1	SG2	SG3	SG4	SG5	SG6	SG7
NAME	AMPLITUDE REGISTER (M.S.BYTE)	AMPLITUDE REGISTER (L.S.BYTE)	FREQUENCY MANTISSA (M.S.BYTE)	FREQUENCY MANTISSA (L.S.BYTE)	FREQUENCY EXPONENT	HARMONIC REGISTER	END PHASE	BIAS REGISTER
TYPE	← WRITE ONLY →							
BOARD	GENERATOR D-A		GENERATOR CONTROL			GENERATOR D-A		
LATCH	1A	4A	7C	5C	11B	10B	8A	6A
FORMAT	BIT	FUNCTION						
	7	WAVE SHAPE	M.S.B. ↑	M.S.B. ↑	M.S.B. ↑	RESERVED	NOT USED	ENABLE ↑
	6							
	5	OUTPUT RANGE	D A T A ↑	D A T A ↑	D A T A ↑	M.S.B. ↑ BINARY POINT VALUE	1st HARM FLAG	PHASE
	4						NOT USED	
	3						M.S.B. ↑ HARMONIC VALUE	NOT USED
	2	R.M.S. / PEAK	L.S.B. ↓	L.S.B. ↓	L.S.B. ↓	L.S.B. ↓	L.S.B. ↓	BIAS SIGN
	1	M.S.B.						BIAS M.S.B.
	0	2ND M.S.B.						BIAS 2ND M.S.B.
			L.S.B.	L.S.B.	NOT USED	L.S.B.	L.S.B.	L.S.B.



GENERATOR CONTROL BOARD FIG. 6-3-2

Introduction

The function of the Generator Digital-to-Analogue Board is to generate an analogue output signal which is at the frequency defined by the Fundamental frequency input from the Generator Control Board, and which possesses the waveshape, amplitude, phase and d.c. offset characteristics specified by data inputs from the Microprocessor. Provision is made for synchronising the signal to a signal obtained from a source external to the F.R.A.

A block functional diagram of the board is shown in fig.6.4.1 (E82035) or fig 6.4.2 (E88662).

OPERATION

Circuit Isolation

Operational considerations require all the board's circuits other than the interface registers and the Output Amplifier to be isolated from earth. This is achieved by 'floating' the power supplies for the devices concerned and by using opto-isolators for the exchange of data and control signals between them and 'earthy' areas of the system.

Interfacing

The board interfaces with the System Data Bus via the four interface registers IC1A, IC4A, IC6A and IC8A. At 'power on', the registers are cleared by the INTL (INITIALISE) signal from the Processor and Cursor Control Board. At all other times the interface is controlled by the SELECT GENERATOR signals SG0, 1, 6 and 7; these signals are generated as described in Chapter 6.3, which also contains complete details of the registers.

Pulse Synchroniser

This circuit enables the positive-going, zero-crossing point of the GENERATOR OUTPUT signal to be synchronised with a squarewave EXT SYNC. signal, obtained from an external source via the External Sync. Control Board. The circuit's action is summarised in fig. 6.4.1; the effect of the circuit's output upon the operation of the counter to which it is applied is described in the subsection which follows.

10-Bit Programmable Counter

Under the control of the inverted FNDL (FUNDAMENTAL) signal, the 10-Bit Programmable Counter counts up through 1024 steps for each cycle of GENERATOR OUTPUT. Thus bit 9 of the counter gives the polarity of the output waveform and represents the m.s.b. of the waveform phase at any instant. Hence the 10-bit phase advances

$\frac{360^\circ}{1024} (\approx 0.35^\circ)$ at each rising edge of FNDL.

When the F.R.A. is operating in the 'internal sync.' mode, no $\overline{\text{LOAD}}$ signal inputs are applied to the counter, and thus it continuously cycles through the 0 to 1024 count sequence and is unaffected by the logic levels present at the parallel inputs to the device.

When the 'external sync.' mode is in use, each rising edge of the sync. signal results in a $\overline{\text{LOAD}}$ pulse being applied to the counter as previously described, presetting the counter to the count of two defined by its parallel inputs (a count of two rather than of zero must be set in because the $\overline{\text{LOAD}}$ pulse effectively disables the counter for one $\overline{\text{FNDL}}$ pulse, and the inherent circuit delays result in the counter also being unable to respond to the $\overline{\text{FNDL}}$ pulse which immediately follows the $\overline{\text{LOAD}}$ pulse). In this mode, the frequency of the F.R.A. output signal is always that of the external sync input. Thus each EXT SYNC. period contains 1024 $\overline{\text{FNDL}}$ pulses and hence the $\overline{\text{LOAD}}$ pulse ensures that the start of each cycle of GENERATOR OUTPUT is referred to the same point in the EXT SYNC. signal.

Waveform Synthesis

The required output waveshape (square wave, sine wave or triangular wave) is defined by program via bits 7 and 8 of the Amplitude L.S. Byte interface register. These bits provide the internal signals DS2^* and $\overline{\text{DS1}}^*$, respectively, which are used to select the source of the 8-bit magnitude input to the Waveshape Digital-to-Analogue Converter (D.A.C.) in accordance with the waveshape to be generated. The sign bit input to the D.A.C. is always provided by the polarity bit (bit 9) of the 10-bit Presettable Counter.

Irrespective of the waveshape selected, the magnitude and polarity bits are latched before being applied to the D.A.C., in order to eliminate analogue spikes caused by differences of speed between the counter output bits and those of the Sine Lookup Table. Latching occurs on the rising edge of $\overline{\text{FNDL}}$, and thus the D.A.C. output follows the counter by one $\overline{\text{FNDL}}$ period ($\frac{360^\circ}{1024}$).

Square Wave Generation. To demand a squarewave, DS2^* and $\overline{\text{DS1}}^*$ are both made logic high, disabling the Sine Lookup Table and the Function Magnitude Buffer. Thus the 8-bit byte P0^* to P7^* representing the magnitude input to the D.A.C. is pulled to logic high, causing the D.A.C. output to alternate between maximum positive amplitude (sign bit high) and maximum negative amplitude (sign bit low) with a period equal to $1024 \times \text{period of } \overline{\text{FNDL}}$.

Sine Wave Generation. The sine waveshape is selected by making DS2^* and $\overline{\text{DS1}}^*$ both low, thus enabling the Sine Lookup Table. This is a 256-word $\times$ 8-bit PROM which is pre-programmed with a sine lookup table for 8-bit address values from 0° to 90° , the table contents being calculated as follows.

Address	Angle (degrees)	Location Contents
L L L L L L L L	$\frac{90}{512}$	$\sin \left(\frac{90}{512} \right)$
L L L L L L L H	$3 \times \frac{90}{512}$	$\sin \left(3 \times \frac{90}{512} \right)$
L L L L L L H L	$5 \times \frac{90}{512}$	$\sin \left(5 \times \frac{90}{512} \right)$
A	$\frac{A \times 90}{256} + \frac{90}{512}$	$\sin \left[\frac{90}{512} (2A + 1) \right]$
H H H H H H H H	$\frac{511}{512} \times 90$	$\sin \left(\frac{511}{512} \times 90 \right)$

(The sine output is modified by the additional $\frac{90^0}{512}$ to eliminate zero-crossing distortion).

However, in the present application the Lookup Table is required to be capable of supplying values of sine for the range of angles between 0^0 and 360^0 . To enable this requirement to be met, each of counter bits 0 to 7 passes to its respective PROM input via an Exclusive Or-gate, which also receives counter bit 8. This results in the address being inverted during quadrants that contain decreasing values of sine, as shown below.

Quadrant Bit 8 Bit 9		Sine Wave Polarity	Angle Range	Address Normal/Inverse
0	0	+	0^0 to 90^0	Normal
0	1	+	90^0 to 180^0	Inverse
1	0	-	180^0 to 270^0	Normal
1	1	-	270^0 to 360^0	Inverse

Triangular Wave Generation. Since PHASE byte P0 to P7 changes in single binary steps clocked by the rising edge of FNDL, and effectively counts up and down on alternate quarter cycles, by applying the byte directly to the D.A.C. a triangular wave output can be produced. This is achieved by means of selection code DS2* high, DS1* low, i.e. by enabling the Function Magnitude Buffer.

Output Amplitude Control

The amplitude of the GENERATOR OUTPUT signal is defined by:

(a) AMPLITUDE bits A0* to A9*,

- (b) the RMS/PK-PK* bit,
- (c) RANGE SELECT bits RS0* to RS2*,
- (d) the gain of the analogue Output Amplifier

Items (a) to (c) inclusive are set and reset by program and input via the Amplitude M.S. Byte and Amplitude L.S. Byte interface registers.

A0 to A9* Control.* A0* to A9* provide the 'magnitude' inputs of the Amplitude D.A.C. The sign bit of this D.A.C. is held high from its reference output and thus the analogue output of the device is always within the range 0V to +10V.

RMS/PK-PK Control.* The analogue output of the Amplitude D.A.C. is passed to the reference input of the Waveshape D.A.C. via the RMS/PK-PK Scaling circuit. Thus the output of the latter determines the maximum positive and negative values of the Waveshape D.A.C. according to whether RMS (bit high) or PK-PK (bit low) is demanded (it should be noted that the RMS scaling is calibrated for use with sinewave output only).

RS0 to RS2* Control.* The amplitude-adjusted waveform from the Waveshape D.A.C. enters the analogue Output Amplifier via an f.e.t. switch-selected attenuator network operated by RANGE SELECT bits RS0* to RS2*, these bits adjusting the amplifier input signal amplitude as required to enable the demanded GENERATOR OUTPUT voltage range to be attained. The output range selection codes are as shown below:

Output Range (V)	RS2*	Bit RS1*	RS0*
0.313 to 9.99	H	H	L
0.032 to 0.312	H	L	H
0.001 to 0.031	L	H	H

Output Amplifier. The analogue Output Amplifier is a 3-stage amplifier with an approximate overall gain of ÷100, ÷10 or x1, depending on the setting of the input attenuator. A programmed d.c. bias can be introduced into the output via the second stage, which also incorporates the preset potentiometer used to null the bias under static conditions.

Manual Bias Selection (E88662 only). The bias setting potentiometer on the control panel via IC1E provides a manually set d.c. offset for the generator output. Relay RLA operated by the MANUAL/AUTO switch on the control panel in the MANUAL position selects the manually set bias level instead of the programmed bias level from IC6C for the output.

Generation of Programmed Bias

The value and polarity of the d.c. bias injected into the GENERATOR OUTPUT is defined by the 11-bit BIAS byte B0* to B10*, set by program and input to the board via the Bias and End Phase interface registers. These bits provide the 'magnitude' (10 bits) and sign (1 bit) inputs to the Bias D.A.C., which therefore generates the d.c. analogue of the magnitude bits at the polarity defined by the sign bit.

End Phase Facility

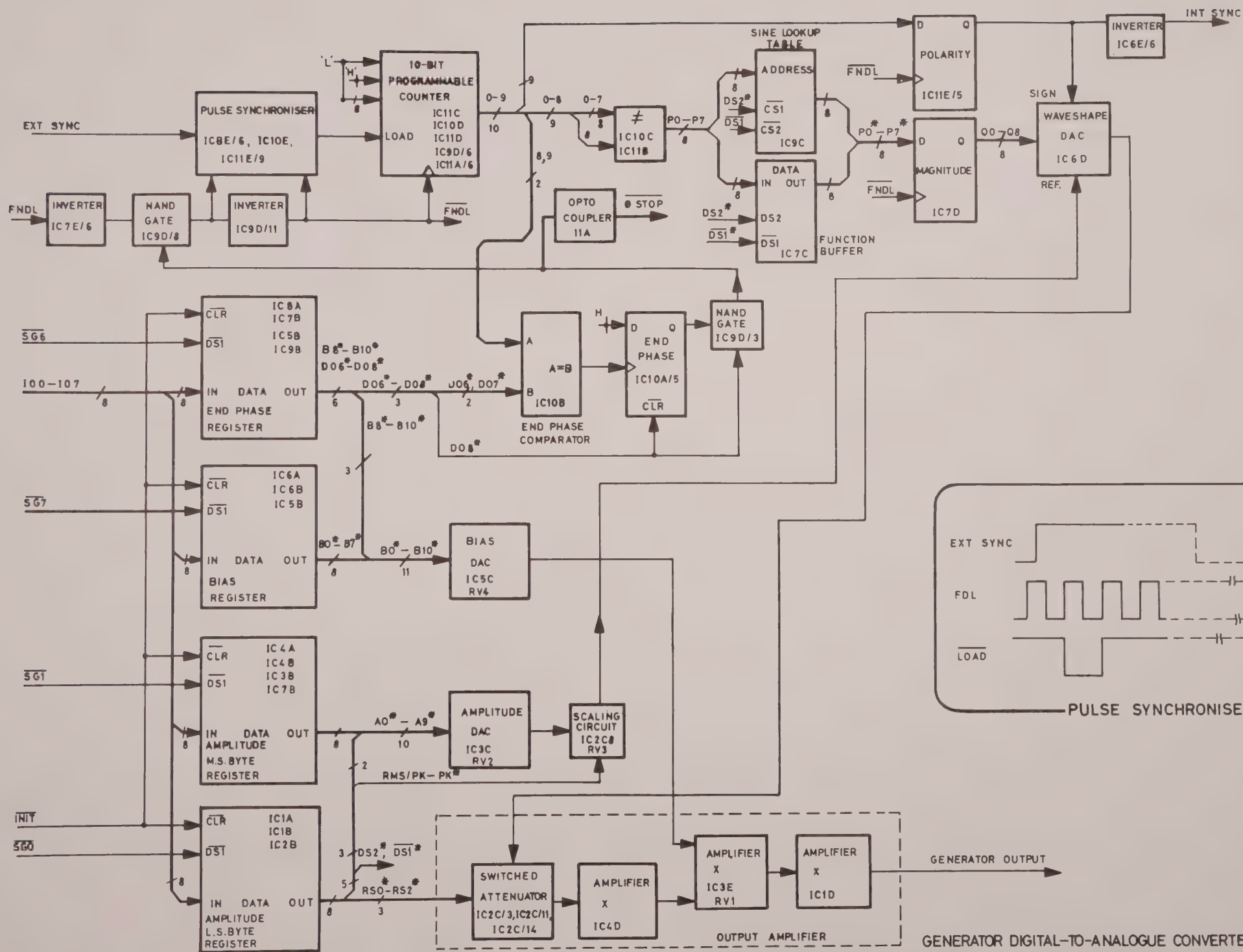
The end phase facility enables the waveform synthesiser to be halted on next reaching a specified quadrant in the output waveshape, thus 'freezing' the GENERATOR OUTPUT at the phase angle.

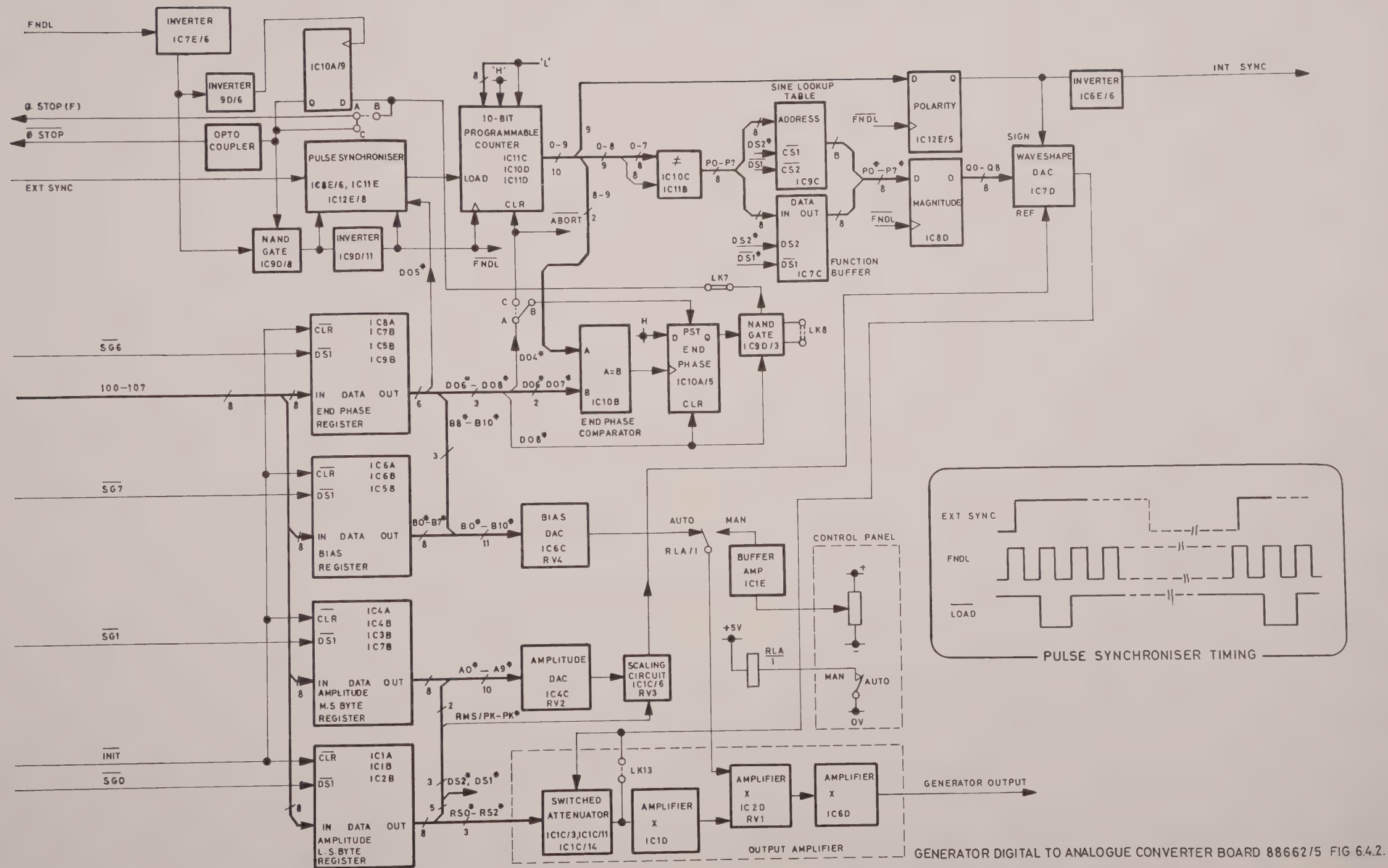
The end phase data and control is contained in the three m.s.b. of the End Phase interface register - i.e. bits D08*, D07* and D06*. Bit D08* high enables the facility by enabling the End Phase latch and Nand-gate IC9D/3. Bits D07* and D06* are constantly compared with counter bits 9 and 8 respectively. When the phase next reaches the value indicated by D07* and D06* (see Sine Wave Generation), the End Phase Comparator outputs a logic high. The rising edge of this output sets the End Phase latch and hence the output of Nand-gate IC9D/3 becomes low, inhibiting further input of FNDL pulses by inhibiting Nand-gate IC9D/8. Thus the 10-bit Counter sequence is halted, halting the GENERATOR OUTPUT at the demanded phase. The output of IC9D/3 is also passed to the Correlator as Φ STOP, via opto-coupler IC11A (IC10E on E88662).

The Generator function is restarted by returning D08* low. It will then automatically resynchronise to EXT SYNC if that signal is present.

Int Sync Output

In addition to its use in the generation of the output signal, counter bit 9 (the polarity bit) is also output to the Correlator as signal INT SYNC, used to phase lock the correlator circuits to the F.R.A. output signal.





GENERATOR DIGITAL TO ANALOGUE CONVERTER BOARD 88662/5 FIG 6.4.2.

CORRELATOR CONTROL BOARD

CHAPTER 6.5

Introduction

The Correlator Control Board:

- (a) Provides an interface for the exchange of data and control signals between the Correlator and Microprocessor functions.
- (b) Provides part of the arithmetic processing necessary to perform signal correlation and signal averaging.
- (c) Enables the sine and cosine products obtained during correlation and averaging operations to be accumulated prior to their onward transmission to the Microprocessor and the Memory.

An overall block diagram of the board is shown in fig. 6.5.1; detailed functional block diagrams of individual areas of the board circuits are given as indicated in the text.

OPERATION

Interfacing (fig. 6.5.2)

The Vector Address Comparator constantly monitors the System Address Bus bits ADD3 to ADD7. When the value of these address bits equals the value set in at the Address Selector switch array, i.e. when the address on the Bus is within the range of vector and port addresses allocated to the particular correlator channel (48 Hex. to 4F Hex. for Correlator 1; 60 Hex. to 67 Hex. for Correlator 2), the comparator output goes low. Thus the m.s. input to the Port Address Decoder becomes low and the Bidirectional Bus Driver which interfaces the Correlator Data Bus and the System Data Bus is enabled into the 'receive' mode.

The three l.s. inputs to the Port Address Decoder are provided by the three l.s.b. of the System Address Bus (ADD0 to ADD2). With the m.s. input high, the decoder outputs which result from this arrangement are outside the range indicated by decoder outputs S0 to S7 (SELECT 0 to 7) and these signals thus remain low. The change of state of the m.s. input to low rectifies this 'out of range' condition and so the SELECT signal defined by ADD0 to ADD2 becomes low, selecting the corresponding interface register (port) as the device to which information will be written - or from which information will be extracted - during subsequent operations. The actual transfer of information is enabled by the IOWM (INPUT OUTPUT WRITE MAPPED) and IORM (INPUT OUTPUT READ MAPPED) signals from the Processor and Cursor Control Board, in accordance with whether the register is a Read/Write, Write Only or Read Only device. Eight interface registers are provided in each correlator channel; details of the registers are given in table 6.5.1 at the end of this chapter.

As indicated above, during the time that the Correlator is addressed the Bidirectional Bus Driver is normally in the 'receive' mode, allowing data to be written to the function. During read operations, the IORM signal input sets the Bus Driver into the 'transmit' mode, to allow data to pass from the Correlator Data Bus to the System Data Bus.

Generation of Serial Product (fig. 6.5.3)

The manner in which the board circuits generate the SERIAL PRODUCT output depends upon whether the correlator function is operating in the Correlate mode or the Average mode, i.e. whether or not bit 5 of the Command Register (Write) is set.

Correlate Mode. During the Correlate mode, SERIAL PRODUCT is obtained by effectively multiplying the SERIAL MULTIPLICAND input from the Correlator Analogue-to-Digital Converter Board by cosine and sine waves at the measurement harmonic frequency.

The HMNC (HARMONIC) input from the Generator Control Board - at 1024 times the selected harmonic signal frequency - is buffered and used to clock the 10-bit, presettable, Address and Quadrant Counter. The counter is maintained in synchronism with the output signal by means of the INT. SYNC. (INTERNAL SYNC.) signal from the Generator Digital-to-Analogue Converter Board, which causes the counter to be reset to a count of one at the start of each cycle of the output signal.

On each rising edge of the SAMPLE STROBE input signal, i.e. when a sample has been taken, the counter outputs are loaded into the Counter State latches; simultaneously, the counter state obtaining at the time the previous sample was taken is transferred into the Table Address and Quadrant latches. The delay which thus occurs between a counter state being staticised and that state being utilised in the multiplication operations and in the production of quadrant information allows time for the Converter Board to process the associated sample into the SERIAL MULTIPLICAND.

The Sine Lookup Table is a 256-word x 8-bit PROM which is internally-programmed to supply the value of sine for angles between 0° and 90° at increments of $\frac{90}{256}$ (i.e. $0.3516^\circ/\text{word}$). However, the present application of the PROM requires that it be capable of supplying values of both sine and cosine for the range of angles between 0° and 360° . To enable this requirement to be met, each address line is connected to its respective PROM input via an Exclusive Or-gate, which also receives the exclusive or of the SAMPLE STROBE signal and the staticised quadrant bit A. This results in the address being inverted during quadrants that contain decreasing values of sine or cosine.

In addition to its use in the modification of the PROM address, quadrant bit A is passed to the board output as QUADRANT signal QD2. Also, it is gated (Exclusive Or) with the associated quadrant bit B and the resultant made available as board output QD1. Signal QD1 gives the polarity of the cosine wave, while QD2 gives the polarity of the sine wave; in either case, logic high indicates negative polarity.

The 8x1-bit output of the Lookup Table is Anded with the SERIAL MULTIPLICAND to provide partial products, which are then summed in the adder using the 'shift and add' technique. The Multiplier thus formed by the gates, the adder and the latches is clocked by the MULTIPLIER STROBE signal, which consists of 28 pulses occupying the last 28 time intervals of each of the two 32-interval sequences into which each processing cycle is divided; it is cleared at the start of each 32-interval sequence by MULTIPLIER CLEAR. The SERIAL PRODUCT output of the multiplier is obtained from the adder, l.s.b. first.

Average Mode. With the Average mode commanded, bit 5 of the Command Register (Write) is reset. Thus the Counter State, Quadrant and Table Address latches are maintained clear. This means that the incoming SERIAL MULTIPLICAND is multiplied by a constant instead of a sine or cosine wave. If the samples are uniformly disposed about the zero volt level, then the sum over a complete cycle of the F.R.A. input signal is zero. If, however, there is a d.c. displacement of the signal, then the sum is not zero and its magnitude indicates the size of the displacement. The Microprocessor can thus calculate the value of the displacement and cause a compensating offset to be applied in the correlator input stage.

Accumulator (fig. 6.5.2)

The SERIAL PRODUCT is passed to the Correlator Analogue-to-Digital Converter Board, where it is further processed to obtain the COMMON SUM input for the present board. Here it is clocked into the m.s.b. of the Sine and Cosine Sum Shift Registers by the associated strobe signal, SINE STROBE or COS STROBE (fig. 6.5.4); simultaneously, the previously loaded sine or cosine partial sum is shifted out of the l.s.b. of the clocked register and returned to the Converter Board.

The 8-bit presettable counter which forms the Fraction Register is clocked at the end of each SAMPLE STROBE period. The counter is capable of counting up to 256 samples, the precise number being set by program control. When the limit is reached, the counter outputs an OP LATCH pulse which causes the contents of the Sum Shift Registers to be latched into the Sine Product and Cos Product interface registers; also, if interrupts are allowed, an interrupt request is initiated and the Done bit (bit 0 of the Command Register (Read)) is set, as described later.

Signal OP LATCH is half one SAMPLE STROBE beat in duration. One micro-second after it is generated, the RESET input to the board becomes high for the same duration. Hence on the rising edge of OP LATCH, the Sum Clear latch generates a 1µs low to be presented to the Clear inputs of the Sine and Cosine Sum Shift Registers and the Overflow latch. Thus the registers are cleared and await the next series of partial products, and the overflow indication (if present) is removed.

The registers and the latch are also cleared in response to a Load input to the Fraction Register. Thus whenever the program causes IOWM and S3 to be generated simultaneously, to write a new sample count limit to the Fraction Register, any accumulated partial sums are erased and an overflow indication is removed.

Overflow (fig. 6.5.2)

Overflows are detected at the Correlator Analogue-to-Digital Converter Board. When eight such conditions are discovered during any one Fraction Register count sequence, the OVFL (OVERFLOW) input to the Control Board is made high, causing the Overflow latch to set. The indication of overflow thus provided by the latch output is strobed into bit 8 of the Command Register (Read) by the subsequent OP LATCH pulse.

The Overflow latch is cleared as described in the preceding subsection. The OVFL input is cleared by the OVFLO CLR output of the Fraction Register shortly before OP LATCH.

Interruptions (fig. 6.5.2)

If interruptions are enabled, i.e. if bit 6 of the Command Register (Write) is set, the falling edge of OP LATCH causes the Done latch to set while the rising edge causes the Interrupt Request latch to set. Thus a high is written into bit 0 of the Command Register (Read) and an INTERRUPT REQUEST (IRQ) is generated.

The Done latch and bit are cleared when the Cos Product (M.S.) interface register has been read.

The Interrupt Request latch is reset by the INTA (INTERRUPT ACKNOWLEDGE) output of the Microprocessor. This signal is generated each time an interrupt request is serviced. Thus to ensure that correlator output data is not lost, the Interrupt Request Select switch array is adjusted so that the request is transmitted over the IRQ7 line, allocating the Correlator the highest interrupt priority level.

Power On Reset (fig. 6.5.2)

When power is first applied to the F.R.A. circuits, a short-duration INTL (INITIALISE) pulse is input to the Correlator Control Board from the Processor and Cursor Control Board. Input buffering provides signal INTL*, which is used to clear all interface registers except the Fraction Register and to preset the Register Clear latch, the output of the latter then clearing the Sum Shift Registers and the Overflow latch. Shortly afterwards, a RESET input is received from the Correlator Analogue-to-Digital Converter Board, so the Register Clear latch resets, allowing normal working to commence.

TABLE 6-5-1 INTERFACE REGISTERS DETAILS

ADDRESS (HEX)	CORR 1	48	49	4A	4B	4C	4D	4E	4F	
	CORR 2	60	61	62	63	64	65	66	67	
SELECT		S0	S1	S2	S3	S4	S5	S6	S7	
NAME		COMMAND REGISTER	INPUT OFFSET M.S.BYTE	INPUT OFFSET L.S.BYTE	FRACTION REGISTER	SINE PRODUCT REGISTER (M.S.BYTE)	SINE PRODUCT REGISTER (L.S.BYTE)	COS. PRODUCT REGISTER (M.S.BYTE)	COS. PRODUCT REGISTER (L.S.BYTE)	
TYPE		READ/WRITE	WRITE ONLY			READ ONLY				
LATCH		1D READ 3D WRITE	CORRELATOR A - D		CORRELATOR CONTROL					
BIT		READ	WRITE	3B	5B	9C 10C	2A	1A	4A	3A
FORMAT	BIT	READ	WRITE	NOT USED	M.S.B.	M.S.B.	M.S.B.	M.S.B.	M.S.B.	M.S.B.
	7	O'FLOW	NOT USED		↑	↑	↑	↑	↑	↑
	6	INTR. ENABLE	INTR. ENABLE		↑	↑	↑	↑	↑	↑
	5	NOT USED	CORR'TE AVERAGE		DATA	DATA	DATA	DATA	DATA	DATA
	4		2ND STAGE GAIN							
	3		RMS/PEAK							
	2	NOT USED	3RD STAGE GAIN	NOT USED	DATA	DATA	DATA	DATA	DATA	
	1									
0	DONE	INPUT ATTEN.	2ND M.S.B.	L.S.B.	L.S.B.	L.S.B.	L.S.B.	L.S.B.	L.S.B.	

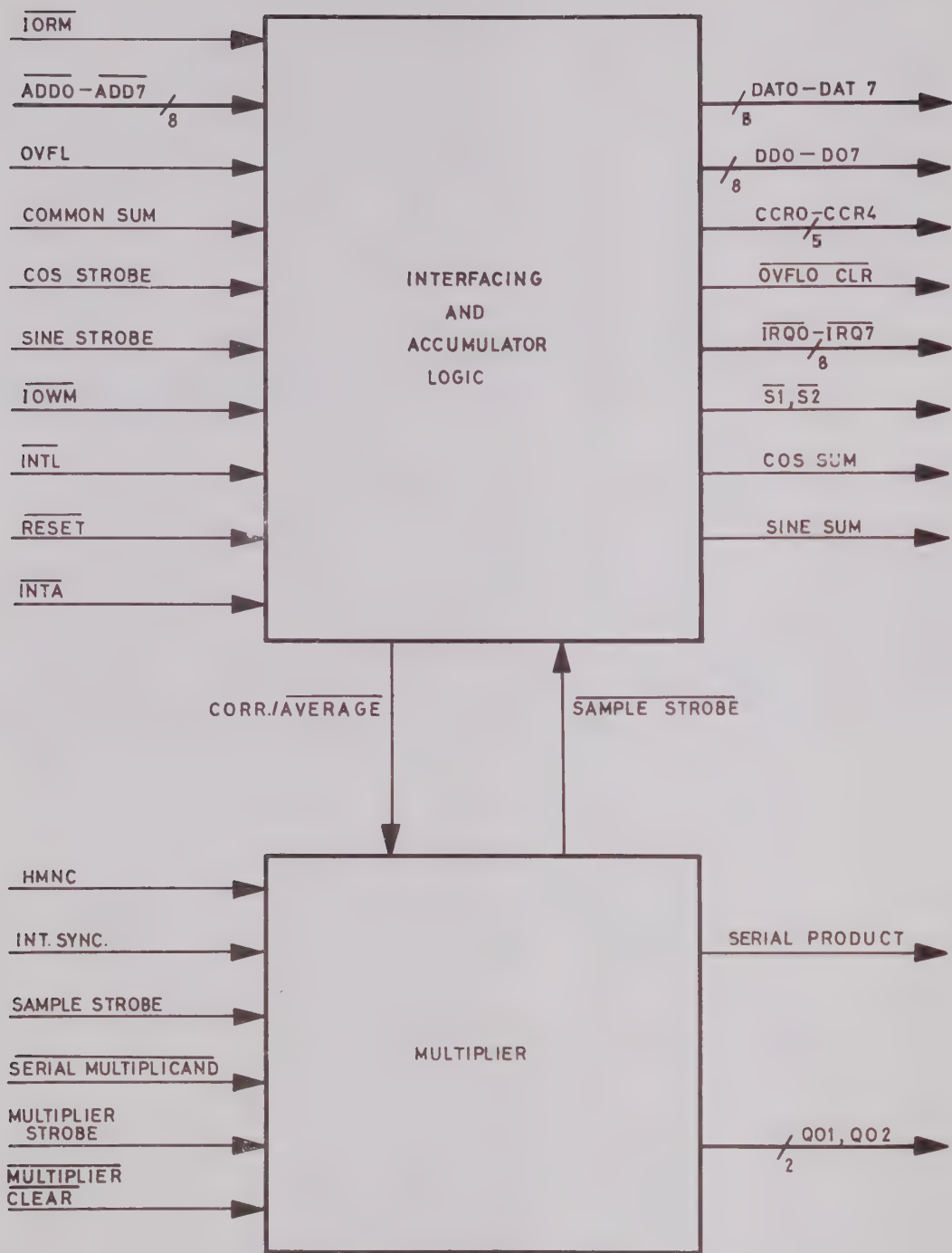


FIG 6.5.1 CORRELATOR CONTROL BOARD B2005/4

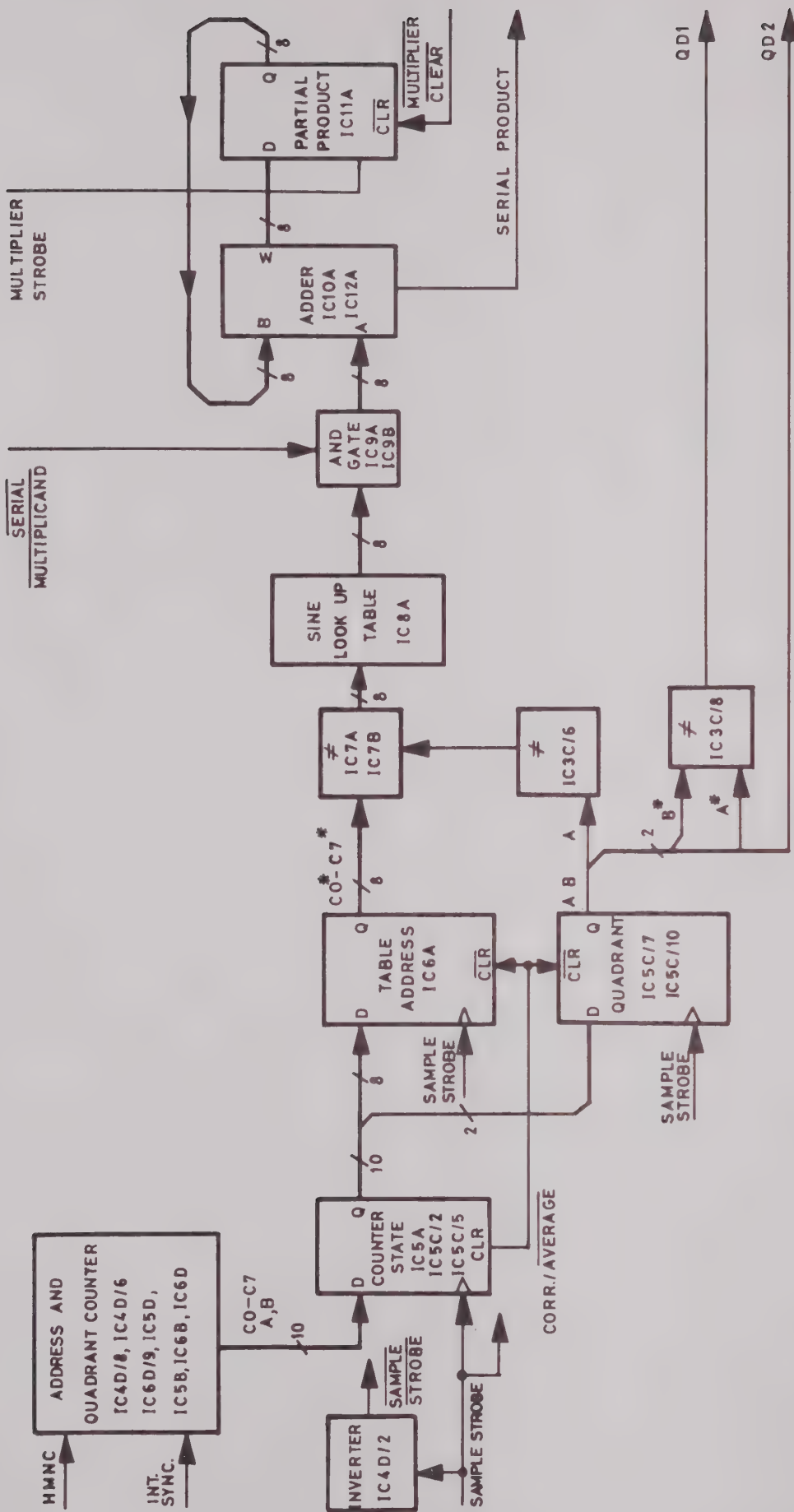


FIG 6.5.3 MULTIPLIER

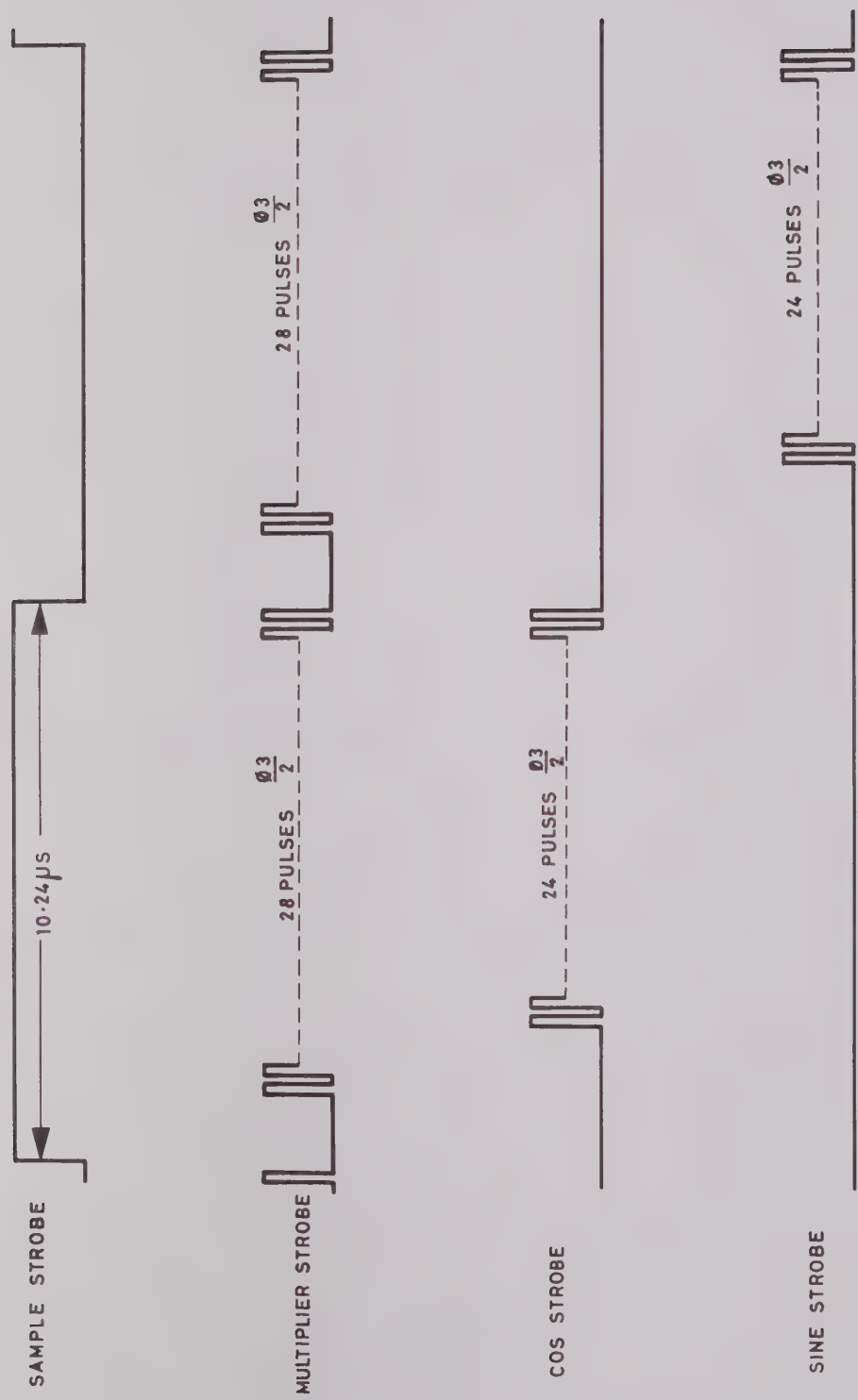


FIG. 6.5.4 STROBE TIMING

CORRELATOR ANALOGUE-TO-DIGITAL BOARD

CHAPTER 6.6

Introduction

The function of the Correlator Analogue-to-Digital Board is to sample the F.R.A. analogue input signal level at the required rate, to convert each of these samples into an equivalent serial digital word and (in conjunction with the Correlator Control Board) to correlate it to the F.R.A. output signal.

An overall functional block diagram of the board is shown in fig. 6.6.1. Detailed functional block diagrams of individual sections of the board circuits are given as indicated in the descriptions which follow.

OPERATION

Circuit Isolation

Operational considerations require the Input Amplifier, the Analogue-to-Digital Converter and certain of the board's control circuits to be isolated from earth. This is achieved by 'floating' the power supplies for the devices concerned and by using opto-isolators for the exchange of data and control signals between them and 'earthy' areas of the system.

Input Amplifier (fig. 6.6.2)

The incoming analogue signal is connected to the Input Amplifier either directly or via a 100:1 attenuator, the path selected being controlled by Correlator Command Register bit CCRO (from the Correlator Control Board) via relays RLA and RLB. Overvoltage protection is provided in the direct path.

The first stage of the 3-stage Input Amplifier is a unity-gain buffer. This presents a high input impedance to the applied signal, thus preventing loading of the input attenuator. The Set Zero Output preset potentiometer is used to null the d.c. offset of the analogue input stages under static conditions.

The second amplifier stage has a gain of unity or $\times 10$, depending upon the value of feedback resistor selected by f.e.t. switches controlled by the CCR4 input to the board. A programmed d.c. bias can be injected into the signal input of the stage to compensate for any d.c. offset contained in the analogue signal applied to the board.

The final stage of the amplifier has a gain of either $\times 2$ or $\times 20$, selected by f.e.t. switches under the control of the CCR2 and CCR3 inputs. The output of the stage is passed to a Sample-Hold circuit via voltage limiting.

Input Ranging (figs. 6.6.2, 6.6.3)

The correlator input range in use is defined by program via Correlator Command Register bits CCRO and CCR4. As indicated in the previous

subsection, bits CCR0 to CCR2 and CCR4 adjust the overall gain of the Input Amplifier. Bit CCR3 adjusts the input level to the Sample-Hold circuit in accordance with whether RMS or Peak value working is commanded. The action of the ranging circuit is summarised below.

Range V	4	3	CCR			Input Attenuator	2nd Stage Gain	3rd Stage Gain
			2	1	0			
500	H	*	L	H	L	÷100	x1	x2
50	L	*	L	H	L	÷100	x10	x2
Special 5	L	*	H	L	L	÷100	x10	x20
5	H	*	L	H	H	÷1	x1	x2
0.5	L	*	L	H	H	÷1	x10	x2
0.05	L	*	H	L	H	÷1	x10	x20

* L = RMS; H = Peak

Generation of Programmed Bias (fig. 6.6.2)

The Correlator Analogue-to-Digital Board interfaces with the System Data Bus via two, Write only, interface registers - the Input Offset M.S. Byte Register and the Input Offset L.S. Byte Register. The microprocessor addresses the registers via the Correlator Control Board, the latter responding to the address by generating the appropriate SELECT signal (S1 or S2). This signal enables the corresponding interface register, and hence the subsequent IOWM (INPUT OUTPUT WRITE MAPPED) pulse from the Processor and Cursor Control Board loads the contents of Correlator Data Bus D00 to D07 - i.e. the contents of the System Data Bus - into the register.

The outputs of the interface registers are coupled to the input of the Digital-to-Analogue Converter, which therefore proceeds to generate a d.c. voltage which is of the value and sign specified by the input offset word currently held in the interface registers.

During the power-on reset sequence, both registers are cleared (and hence the converter output voltage set to zero) by means of the INTL (INITIALISE) signal from the Processor and Cursor Control Board.

Correlator Timing (figs. 6.6.3, 6.6.4)

The analogue signal is sampled at 20.83 μ s intervals, i.e. at a rate of 48 kHz, under the control of the system clock $\Phi 3$. A master timing waveform at this rate (SAMPLE STROBE) is obtained by dividing the $\Phi 3$ system clock input by 128, by means of a Divide-by-Two stage - which provides the internal $\frac{\Phi 3}{2}$ clock - and an Event Sequence Counter.

Each SAMPLE STROBE period therefore corresponds to sixty-four $\frac{\Phi 3}{2}$ clock periods (time intervals). Events occurring within the SAMPLE STROBE

period are timed and synchronised by means of a group of CLOCK ENABLE signals, obtained by suitably decoding outputs from the Event Sequence Counter.

Sampling (figs. 6.6.3, 6.6.5)

The Sample-Hold amplifier enters the 'hold' mode when SAMPLE STROBE goes low and remains in that mode until the STATUS output of the Analogue-to-Digital Converter goes low to indicate that conversion is complete.

Analogue-to-Digital Conversion (figs. 6.6.3, 6.6.5)

One microsecond after the falling edge of SAMPLE STROBE, the Convert Delay outputs a 300 ns CONVERT COMMAND pulse to the Analogue-to-Digital Converter, initiating the conversion process. During the process, the converter STATUS output is high, changing to low when the process is completed.

On completion of conversion the digitised sample becomes available at the parallel data outputs of the converter. This output word is in two's complement format and includes the sign, a positive sample generating a low sign bit and a negative sample a high sign bit.

Shift Register (figs. 6.6.3, 6.6.5)

Shortly after each falling edge of SAMPLE STROBE, the output of the Shift Register Load/Shift Control circuit becomes low for 300 ns. Thus the converter outputs presently applied to the parallel inputs of the register are loaded into the device, subsequently being shifted through the register under the control of $\frac{\Phi 3}{2}$.

The data word is circulated through the register four times during one SAMPLE STROBE period, although in that time it is only used twice - once for the cosine calculations and once for the sine calculations. The word is extracted from the register serially, with the sign bit first followed by the data bits in ascending order of significance.

A pipeline technique is used throughout the processing stages which follow the register. For example, whilst one l.s.b. is being added to the previous results, the next l.s.b. is being multiplied and a third l.s.b. is passing through the Two's Complement-to-Binary Converter.

Generation of Serial Multiplicand (figs. 6.6.3, 6.6.4)

The sample sign bit, available during the first two time intervals within the SAMPLE STROBE period, is clocked into the Sign latch by the rising edge of RESET and thus stored for the remainder of the cosine and sine calculations. During the next eleven time intervals, the data bits are clocked out of the Shift Register and through the Two's Complement-to-Binary Converter, l.s.b. first. If the sign bit is high, signifying a negative sample, the Exclusive Or function inverts the data bits and the 'carry' of the converter is preset high; if the sign bit is low, signifying a positive sample, no inversion of the data bits occurs. The resultant unsigned binary output of the converter is gated out to the Correlator Control Board as the

SERIAL MULTIPLICAND, Nor-gate IC12F preventing further bits passing to the Control Board once the m.s.b. has been clocked through.

Generation of Serial Product (fig. 6.6.3)

The operations performed on the SERIAL MULTIPLICAND at the Correlator Control Board depend upon the Correlator mode of working specified by the program. If the Correlate mode is demanded, SERIAL MULTIPLICAND is effectively multiplied by the cosine wave of the F.R.A. output signal when SAMPLE STROBE is low, and by the sine wave of the output signal when SAMPLE STROBE is high. If the Average mode is demanded, then both SERIAL MULTIPLICAND are multiplied by the same constant. Thus for each sample, two SERIAL PRODUCT data words are returned to the Converter Board.

The multiplication takes place under the control of the MULTIPLIER STROBE signal, a burst of $\frac{\phi 3}{2}$ clock pulses gated through by CLOCK ENABLE 2 to occupy the last twenty-eight intervals of each 32-interval SAMPLE STROBE half period. The multiplier is cleared at the end of each half period by the inverse form of the CLOCK ENABLE (MULTIPLIER CLOCK).

Production of Common Sum (fig. 6.6.6)

The results of previous sample processing, serial COSINE SUM and SINE SUM, and the quadrant sign information appropriate to the current SERIAL PRODUCT, QD1 (cosine) and QD2 (sine), are connected from the Correlator Control Board to the input of the Data Selector. Selection between the two sets of inputs presented is controlled by SAMPLE STROBE, the cosine inputs being selected when that signal is high and the sine inputs when it is low.

During the active period of CLOCK ENABLE 3, the current 8-bit SERIAL PRODUCT is added bit-by-bit to the SELECTED SUM to produce the serial, 8-bit COMMON SUM.

The SERIAL PRODUCT is unsigned. Thus the sign has to be re-inserted and hence the Adder (IC12C) also performs unsigned binary-to-two's complement conversion. The selected quadrant sign is gated with the stored SAMPLE SIGN to give the overall sign of the SERIAL PRODUCT. If the resultant indicates negative sign, the incoming SERIAL PRODUCT is inverted before application to the Add and Carry circuit and the carry of that circuit preset high. If the resultant indicates positive sign, the SERIAL PRODUCT remains unchanged.

The COMMON SUM is loaded into the Cosine or Sine Shift Register at the Correlator Control Board, under the control of the COSINE STROBE or SINE STROBE signal, as appropriate. Each of the strobe signals takes the form of a burst of twenty-four $\frac{\phi 3}{2}$ clock pulses, enabled by CLOCK ENABLE 3 and selected in association with the relevant sum and quadrant signals.

Overflow Detection

Overflow is detected by suitably decoding bits 2 to 4 and the m.s.b. of the Analogue-to-Digital Converter. Each such condition causes the

contents of the Overflow Counter to be incremented by one. Should eight overflow conditions be so recorded during any one set of samples, the fact is indicated to the Correlator Control Board by the OVFL flag.

The counter is reset on completion of each set of samples by the OVFL CLR signal from the Control Board.

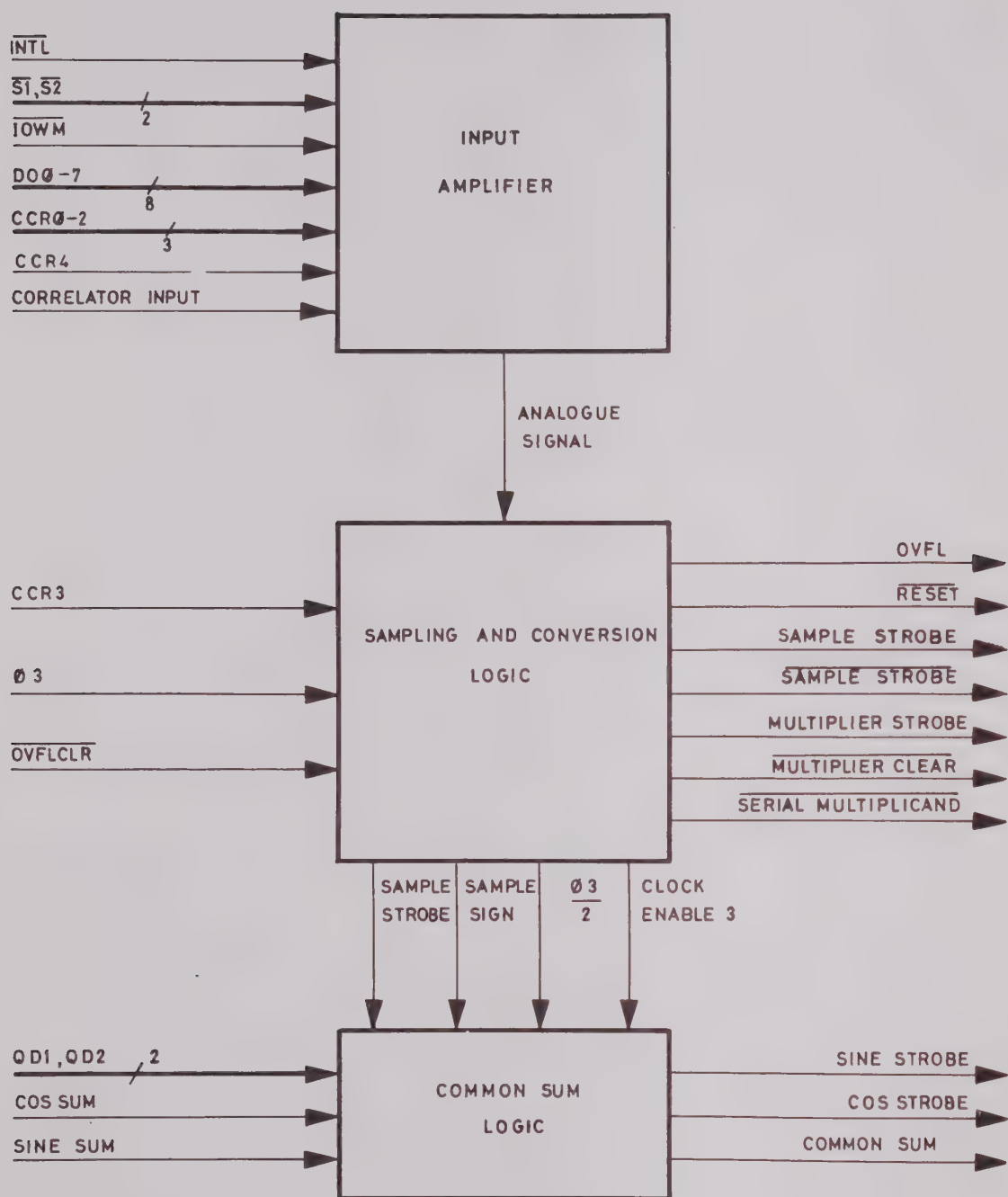
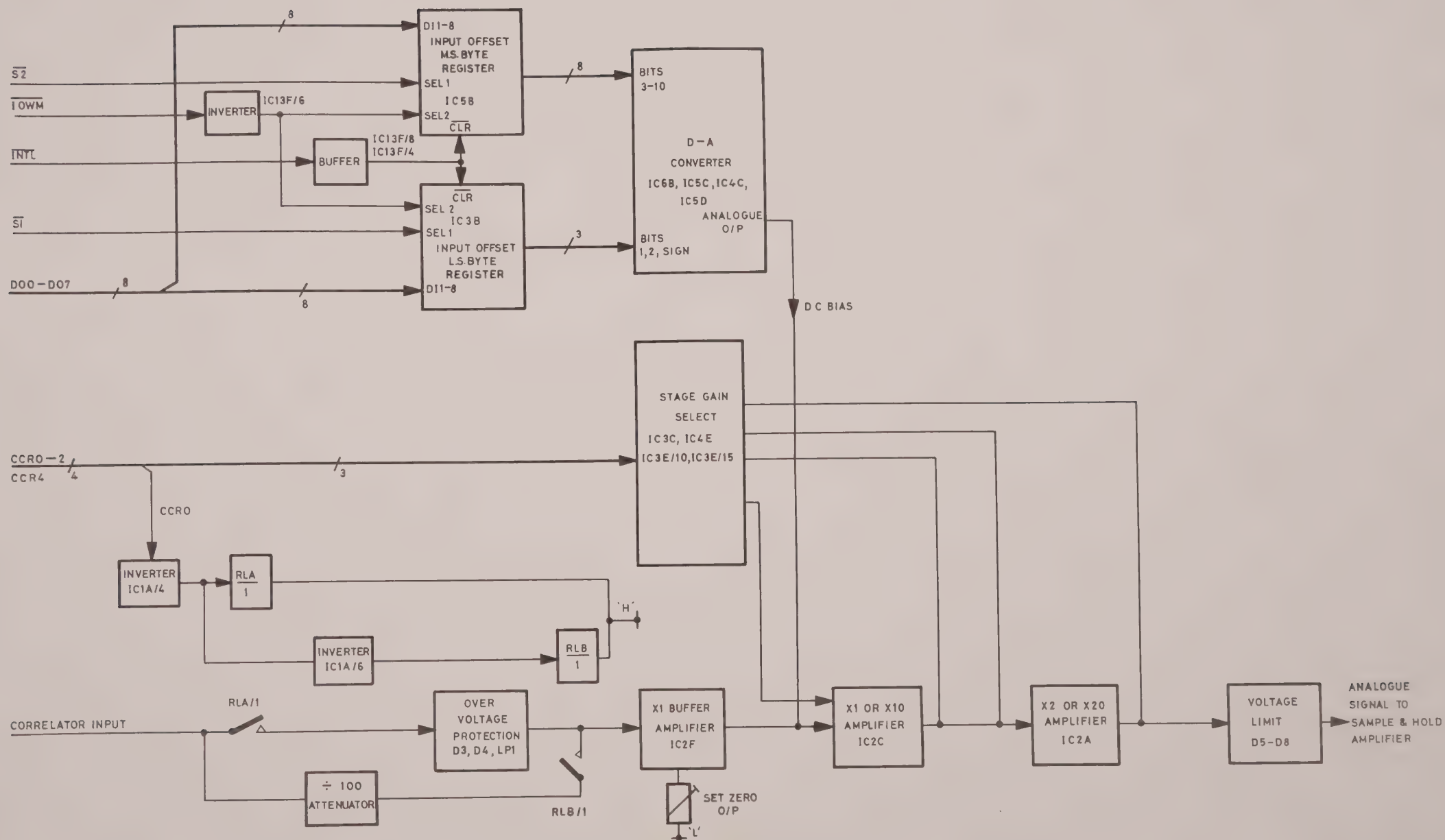
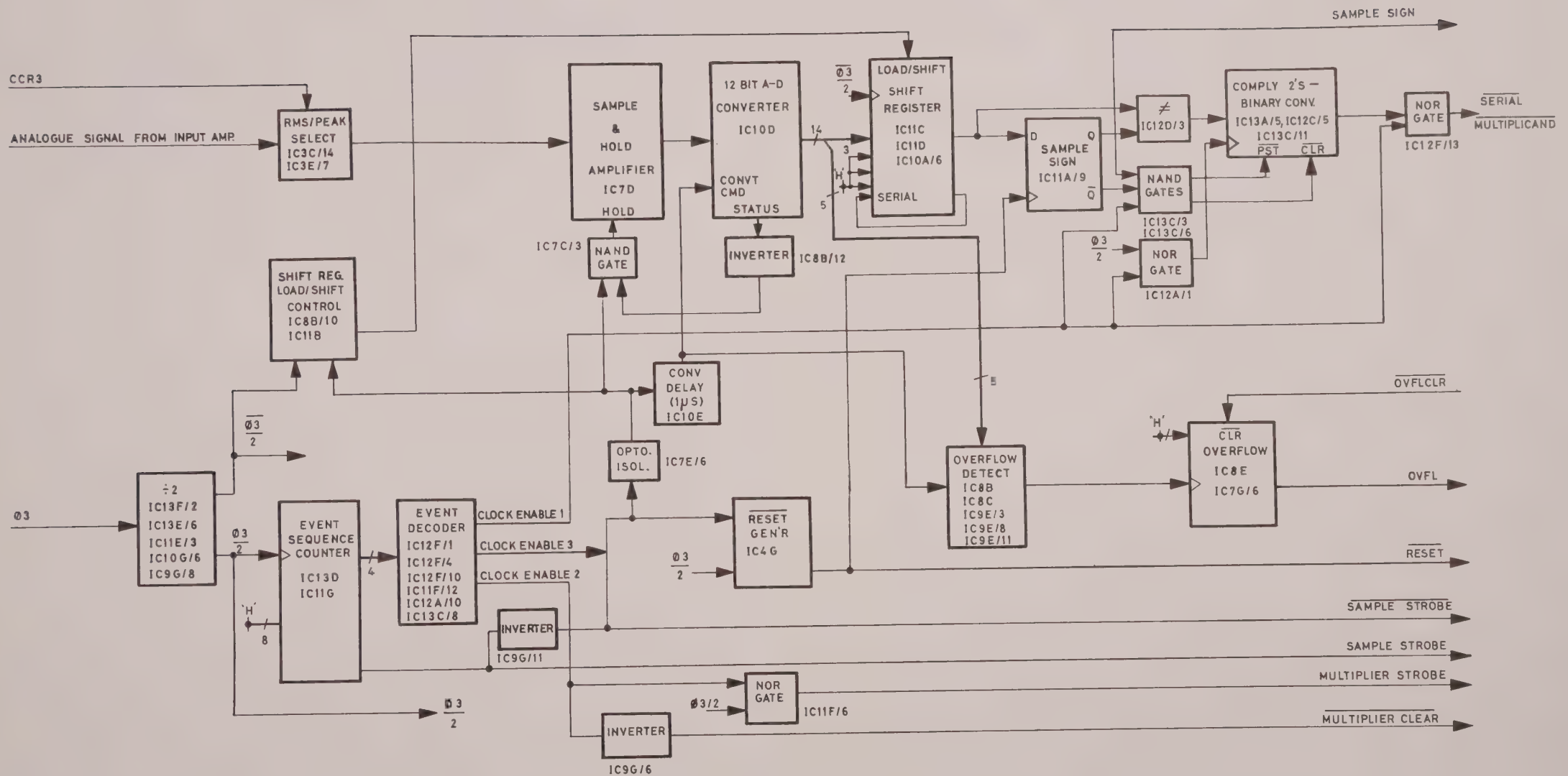


FIG.6.6.1 CORRELATOR ANALOGUE TO DIGITAL BOARD



INPUT AMPLIFIER FIG. 6.6.2



SAMPLING AND CONVERSION LOGIC FIG. 6.6.3

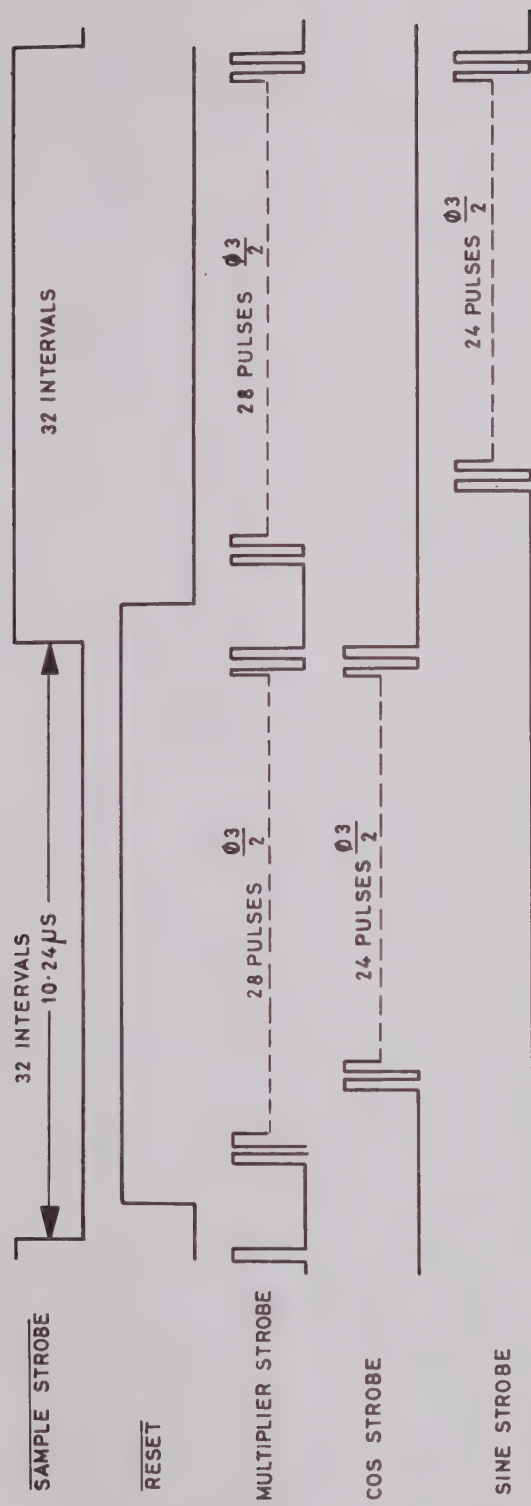


FIG. 6.6.4 CORRELATOR TIMING

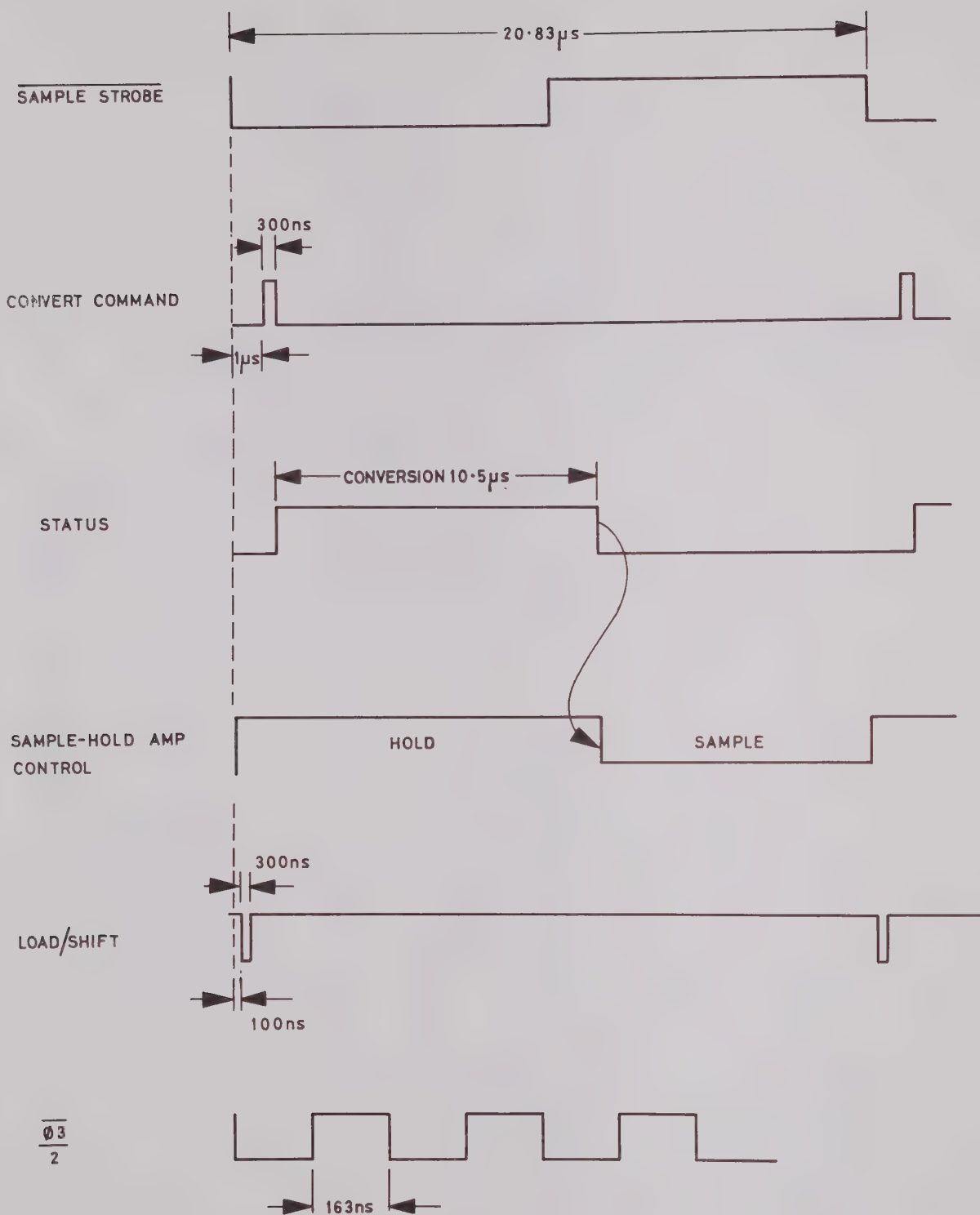


FIG 6.6.5 ADC AND SHIFT REGISTER TIMING

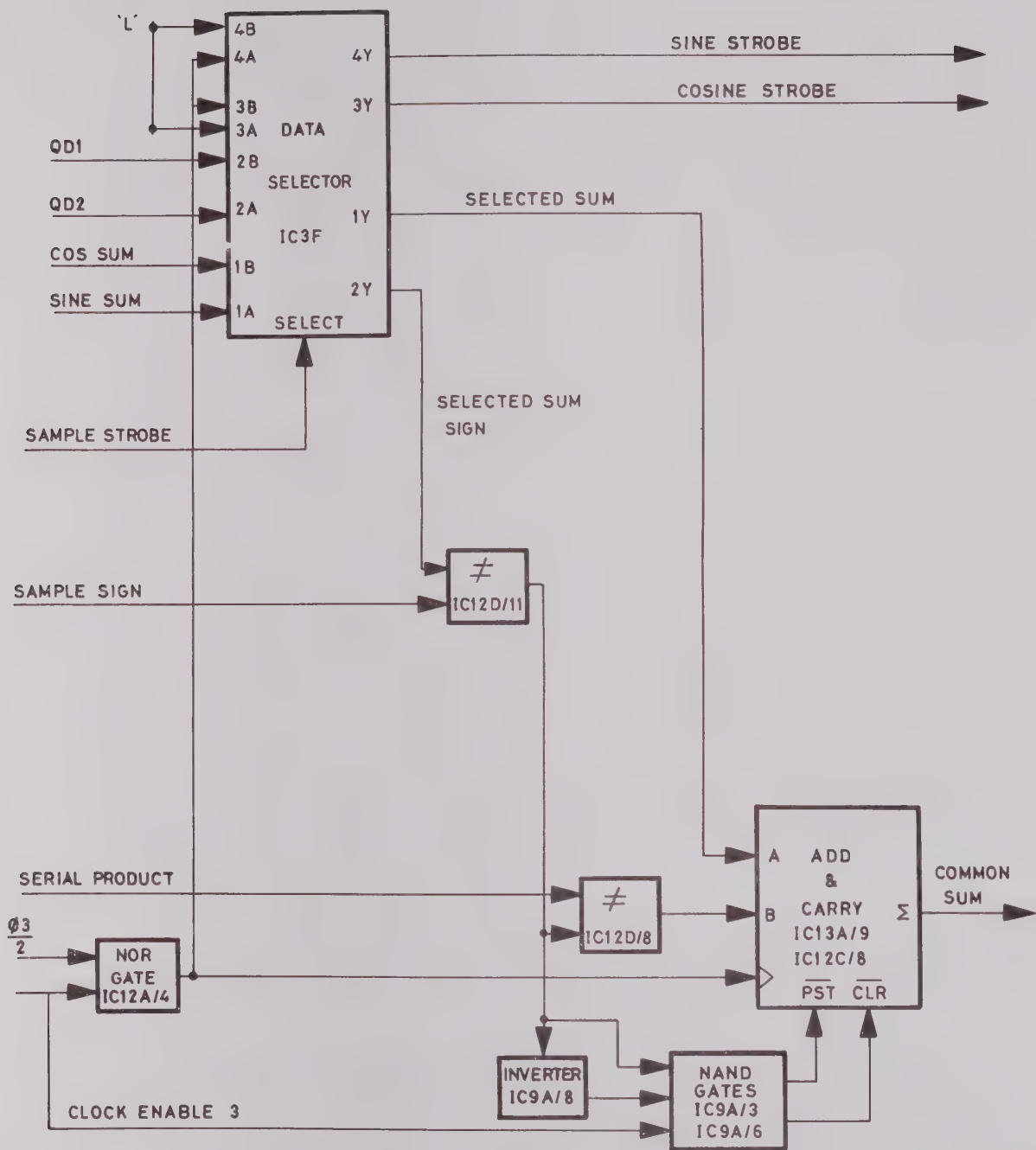


FIG 6.6.6 COMMON SUM LOGIC

DISPLAY CONTROL 1

CHAPTER 6.7

Introduction

Together with Display Control 2, this board provides the waveforms required for the display of alphanumeric characters on the Display Monitor and the synchronising waveforms required to provide a stable video display. The Display can accommodate up to 512 characters in a matrix of 32 columns by 16 rows. The area allocated to each character (character cell) contains 16 t.v. scan lines. Normally the character uses only the first nine lines, but for lower-case characters with hangers, the first three rows are not used but the following nine are. The Display may also show double-height characters. The character cell is then doubled to 32 t.v. lines and character rounding is used on double-height characters to improve legibility.

Display Control 1 contains the main timing waveform chain, the video sync. logic, and the row addressing logic required for character generation (character rounding is performed by Display Control 2). A functional block diagram of the board is shown in fig. 6.7.1.

OPERATION

Timing

The relative timing of the various waveforms generated by the board circuits is shown in figs. 6.7.2, 6.7.3 and 6.7.4., to which reference should be made as necessary during the descriptions which follow.

Main Timing Waveform Chain

The 6.144 MHz $\Phi 3$ system clock feeds a dividing chain the outputs from which are encoded to generate the video sync. waveform, e.g. LB (LINE BLANKING). The chain is divided into four stages as shown in fig. 6.7.1. These are:

- (a) a $\div 10$ stage, which provides a character line waveform $\overline{D}$ to feed
- (b) a $\div 39$ stage, which produces t.v. line waveform K to feed
- (c) a $\div 16$ stage, the final output of which has a cycle time equivalent to one data line (a row of characters) period and feeds
- (d) a $\div 18$ stage, which gives a frame line waveform, V or FB (Frame Blanking).

Sync. Generator

This logic produces the waveforms described below.

DX2. This waveform is used during double-height character generation. It is a rectangular waveform which completes one cycle during a character period. Its purpose, and that of its inverse, is to make the Character Rounding Address Generator produce two addresses during

a character period. One address is used to locate the data for the Reference Register while the other locates the data for the Display Register (see table 6.7.2 and Display Control 2). DX2 is generated by waveform $\overline{C}$ Anded with the $\overline{Q}$ output of latch 7E/6, which is set by A during E.

LSL (LINE STORE LOAD). This allows data for one line of characters to pass through the Data latch and into the Recirculating Line Store (see Display Control 2). It is produced by the Anding of N and P in gate 2C/3, giving a waveform which is high for the last four t.v. lines of a character cell.

LB (LINE BLANKING). LB suppresses any video signals at the end of the line period during flyback (see fig. 6.7.2). It is generated by latch 6E/5, which is preset by $\overline{D.K}$ and cleared by $\overline{K.E}$.

LSC (LINE STORE CLOCK). This is used to clock the line data round the Recirculating Line Store (see Display Control 2) during the first twelve t.v. lines of a character cell. It is generated by gating the output of latch 1E/9 (set by $\overline{A}$ during B) through a Nand-gate during $\overline{K}$. This results in a double pulse during each character time. Note that the Recirculating Store is double loaded, i.e. each character is loaded twice.

$\overline{SYNC}$. This signal comprises $\overline{SYNC\ 1}$ and $\overline{SYNC\ 2}$ (line synchronising pulses), and VS and $\overline{VS}$ (vertical synchronising pulses). The negative-going edges are extracted by the Display Monitor circuits for synchronising the oscillator, while the positive $\overline{VS}$ portion is used by the same oscillator. $\overline{SYNC\ 1}$ is the inverse of $\overline{K.G.F}$ while $\overline{SYNC\ 2}$ is $\overline{K.G.F}$; this ensures that after inversion by 4E/6, the two waveforms combined give a negative-going edge at the beginning of Character Period 35. The generation of VS is described below.

$\overline{VS}$ (VERTICAL SYNCHRONISATION). This provides the frame synchronisation for the Display Monitor in the $\overline{SYNC}$ waveform. It is also used by Display Control 2 to clear the DVL (Data Video Level) latches and to preset the latch which generates the X2 waveform at the end of a frame. $\overline{VS}$ is generated by latch 5D/5 and goes low from the end of Data Line 16 to partway through Data Line 17.

$\overline{RR}$ (RESET REFRESH). This is used to reset the D.M.A. (Refresh) Address Counter on the Processor And Cursor Control Board. It is generated by latch 1E/6, which is set at the beginning of Character Period 18 and cleared shortly afterwards by LN6.

Character Size Control

This logic is controlled by waveform X2, which is at high when double-size characters are to be displayed. The waveforms generated (LDR, LDO, CK*, LSL* and $\overline{LSL^*}$) appear at half their normal frequency when X2 goes high. Selectors 3D and 5E are used to achieve this change to half frequency. The waveforms involved are described in the paragraphs which follow.

CK* (CLOCK*). This is either $\Phi 3$ (normal) or $\overline{A}$ (double-height) and is used to clock the Display and Reference Register in the Character Rounding Logic (Display Control 2).

LDD (LOAD DISPLAYED DISPLAY). This is derived from D retimed by A and A retimed by $\Phi 3$ for normal characters. It is an approximate 0.16 μ s, positive-going pulse which occurs during the latter part of D. When double-height characters are required, each alternate pulse is suppressed by gating the original waveform with an $\bar{E}$ waveform. LDD is used to control the loading of the Display Register from the Data Register and the Reference Register from the Character Generator (Display Control 2).

LDR (LOAD DISPLAY REFERENCE). This is derived by Anding B, C and the inverse of A retimed with $\Phi 3$. It is a similar waveform to LDD, with its positive pulse occurring 0.33 μ s before LDD. It is used to load the Data Latch with the Display Character Data from the Character Generator in Display Control 2.

P*. This is either R* or P. R* may change phase and not frequency when X2 is active. It may change from R to $\bar{R}$.

P has a negative-going edge at the beginning of each data line (equivalent to 16 t.v. lines) and is used in the generation of LSL* and ROMEN. It is therefore important to keep the same phase relationship when X2 is active and P* operates at half frequency. If X2 becomes active at the beginning of an even-numbered data line, R has the same phase as P, i.e. they have coincident negative-going edges. If X2 becomes active at the beginning of an odd-numbered data line, R is in anti-phase to P and therefore $\bar{R}$ must be used as P*. Latch 2E/5 and gate 4E/8 are used to ensure that as X2 becomes active, the resultant R* is in phase with P. Selector 3D performs a straight transformation of waveforms K, L, M and N to half frequency, these waveforms are used with P* to generate ROMEN (ROM ENABLE). LSL* and $\bar{L}SL^*$ are the result of Anding P* and N*; these waveforms are used in the control of the Recirculating Line Store and the generation of X2.

Character Rounding Address Generation

Element 9D encodes waveforms L, M, N, P into the numbered (1 to 16) t.v. lines which form the height of one character cell. These line waveforms are then encoded with DX2, $\bar{D}X2$ and R* by a series of gates to give X2R1 to X2R4, which are the row addressing for double-height characters. Table 6.7.2 shows how the row address changes during each t.v. line to give the two addresses (Reference and Display) which are required for character rounding.

Character Row Address Logic

The X2 waveform via 4C selects either the character row address from the Character Rounding Address Generator for double-height characters or waveforms L to P for normal-size characters. If SHIFT is high, signifying that lower-case characters are required, 3C selects the new address waveforms modified by Adder 3B. In order to provide the hangers on certain lower-case characters (e.g. p), the character data must be displayed on an additional three lines below the normal character height. The address is treated as a modulo 16 number; by Adding 13 to this generated address, 3 is effectively subtracted from the row address. For example, if the unmodified address is 8, by adding 13 it becomes 21; however as it is a modulo 16 number the resultant is $21-16 = 5$, i.e. it is equivalent to $8-3$. The shifted and unshifted addresses for normal size characters are given in table 6.7.1. (Note that double-

height characters may also produce shifted and unshifted new addresses).

ROMEN Generation

This waveform allows the row address to provide access to the Character Generator. Latches 3A/5 and 3A/3 generate two waveforms, SRS (Shifted Row Scan) and URS (Unshifted Row Scan). SHIFT selects SRS to form ROMEN when a lower-case character is required or URS when an upper-case character is required. For upper-case characters of normal size, ROMEN is low for the first nine t.v. lines of the character cell. For lower-case characters of normal size, ROMEN goes low from TV Line No.3 to TV Line NO.13.

Waveform L12* (Line 12) resets the latch generating SRS. L12* is used as timing waveform for the CURSOR BIT (CR), which occurs on the twelfth t.v. line of a character cell, in Display Control 2.

Table 6.7.1 x1 Mode Row Addresses

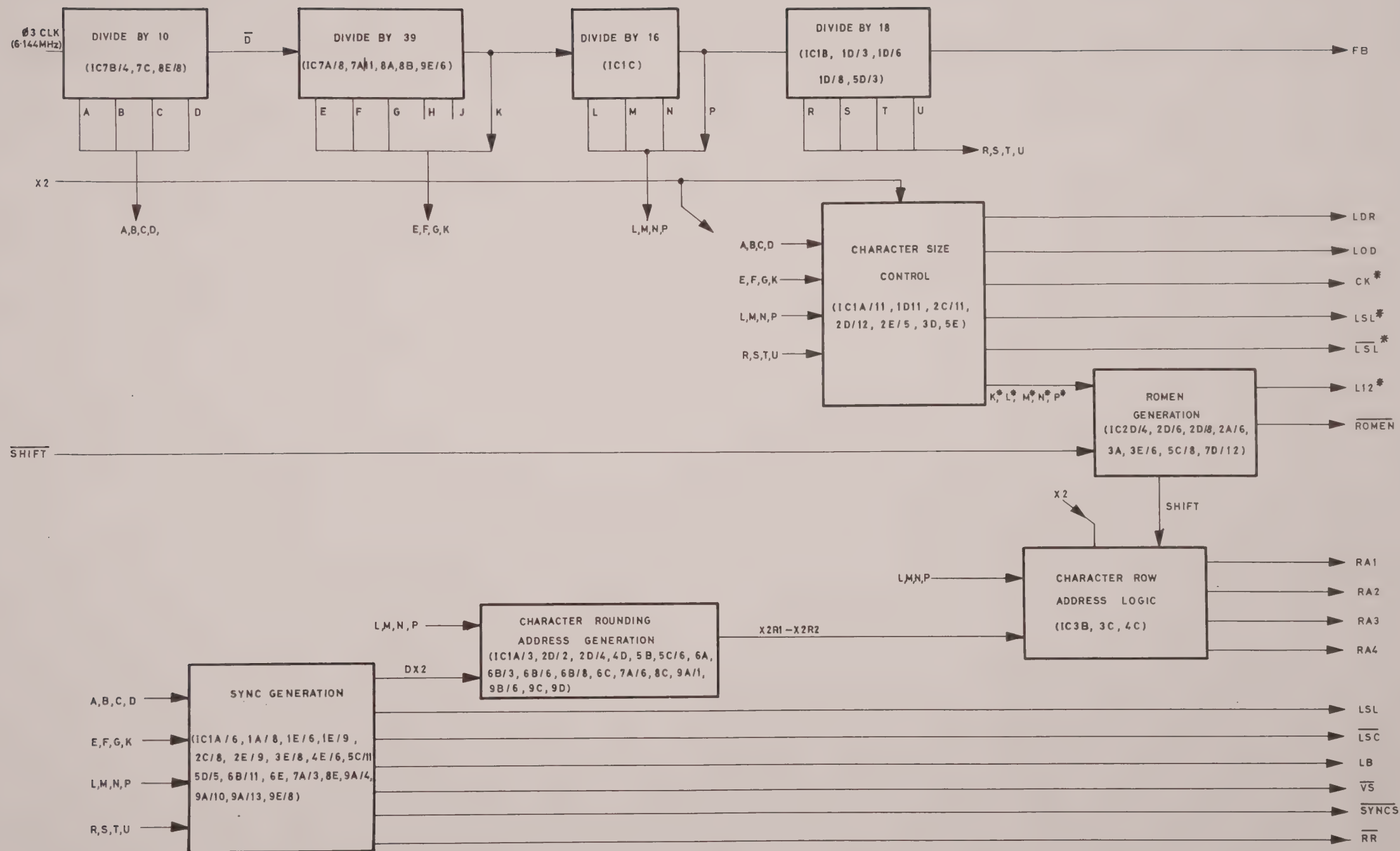
T.V. Line No.	Row Address							
	RA4		RA3		RA2		RA1	
0	0		0		0		0	
1	0		0		0		1	
2	0		0		1		0	
3	0	0	0	0	1	0	1	0
4	0	0	1	0	0	0	0	1
5	0	0	1	0	0	1	1	0
6	0	0	1	0	1	1	0	1
7	0	0	1	1	1	0	1	0
8	1	0	0	1	0	0	0	1
9	1	0	0	1	0	1	1	0
10		0		1		1		1
11		1		0		0		0
12		1		0		0		1
13								
14								
15								

UNSHIFTED

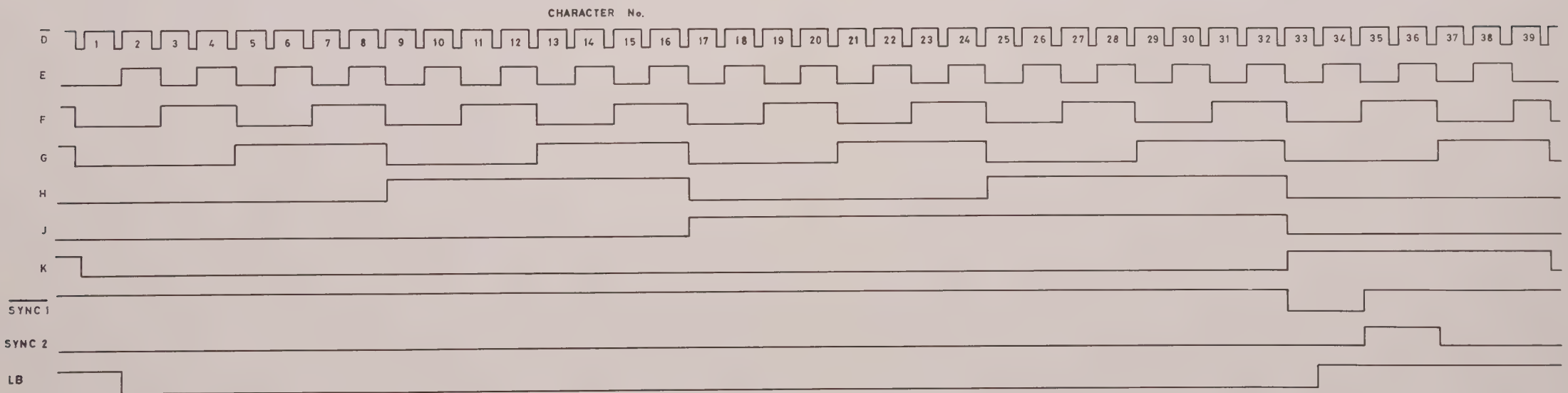
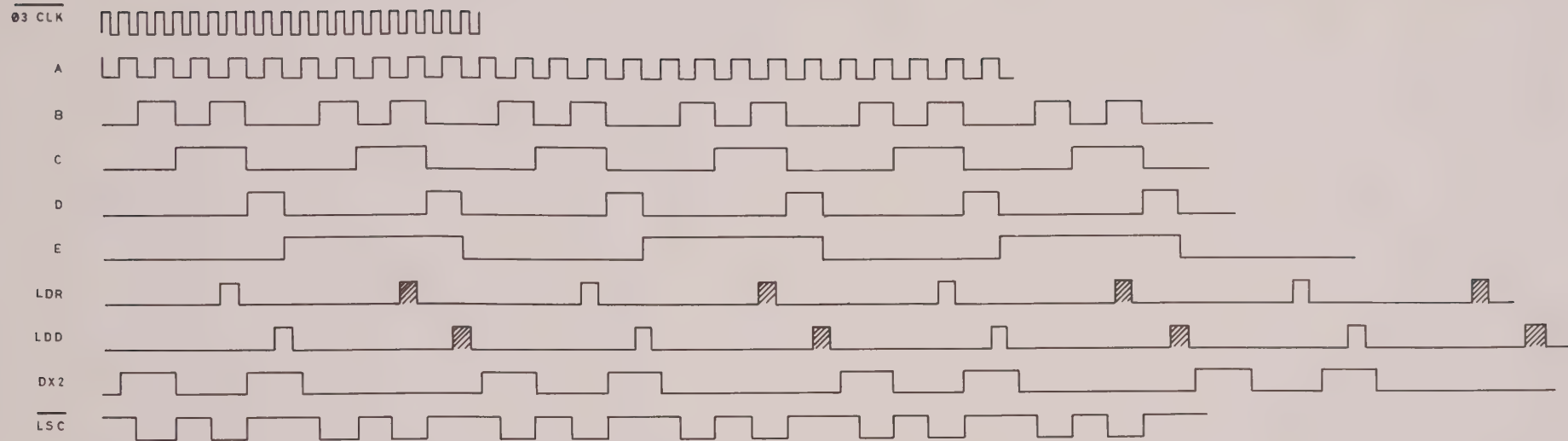
SHIFTED

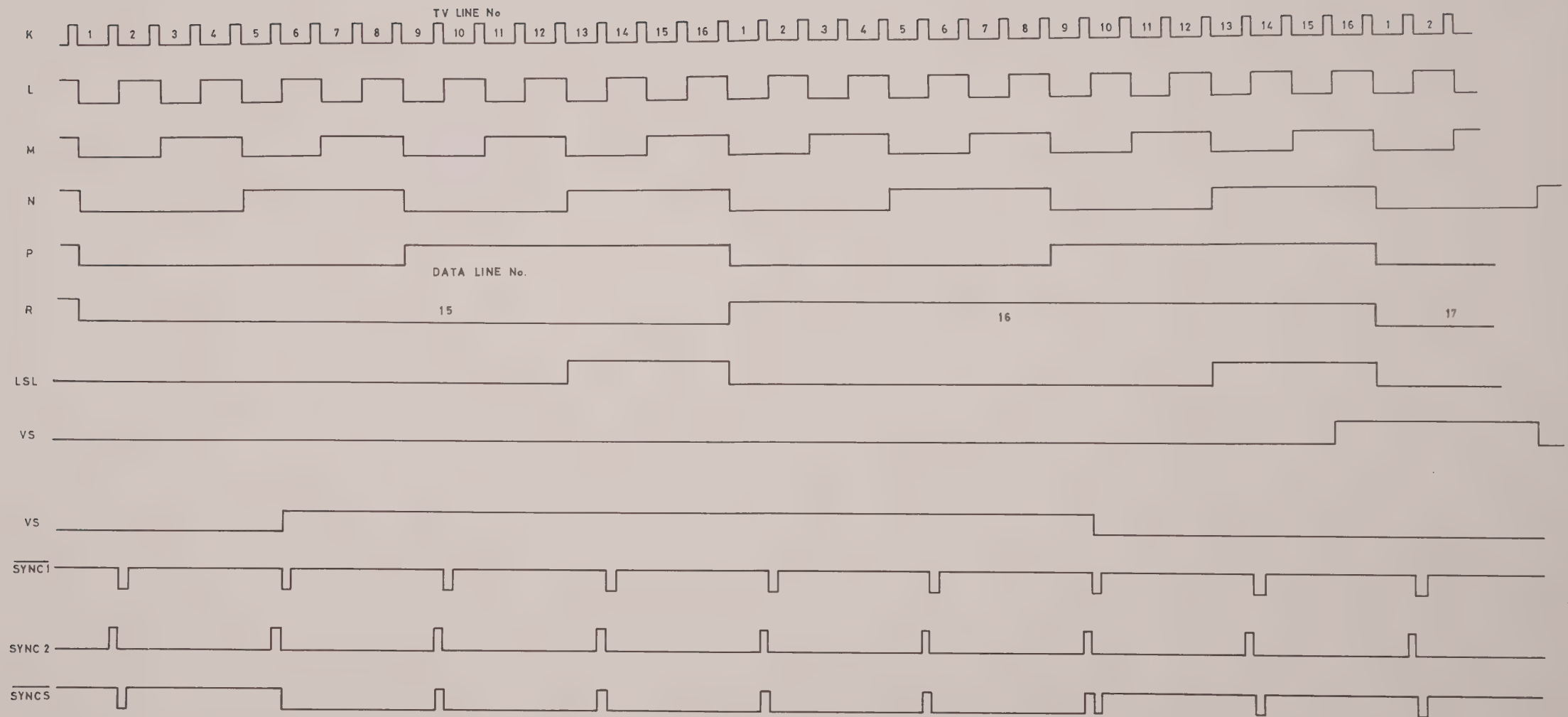
Table 6.7.2 x2 Mode Row Addresses

T.V. Line No.	RA4	Row Address		RA1	Reference Address	Display Address
		RA3	RA2			
0	0	0	0	0	0	0
1	0	0	0	DX2	1	0
2	0	0	0	$\overline{\text{DX2}}$	0	1
3	0	0	DX2	$\overline{\text{DX2}}$	2	1
4	0	0	$\overline{\text{DX2}}$	DX2	1	2
5	0	0	1	DX2	3	2
6	0	0	1	$\overline{\text{DX2}}$	2	3
7	0	DX2	$\overline{\text{DX2}}$	$\overline{\text{DX2}}$	4	3
8	0	$\overline{\text{DX2}}$	DX2	DX2	3	4
9	0	1	0	DX2	5	4
10	0	1	0	$\overline{\text{DX2}}$	4	5
11	0	1	DX2	$\overline{\text{DX2}}$	6	5
12	0	1	$\overline{\text{DX2}}$	DX2	5	6
13	0	1	1	DX2	7	6
14	0	1	1	DX2	6	7
15	DX2	$\overline{\text{DX2}}$	$\overline{\text{DX2}}$	$\overline{\text{DX2}}$	8	7
16	$\overline{\text{DX2}}$	DX2	DX2	DX2	7	8
17	1	0	0	DX2	9	8
18	1	0	0	$\overline{\text{DX2}}$	8	9
19	1	0	DX2	$\overline{\text{DX2}}$	10	9
20	1	0	$\overline{\text{DX2}}$	DX2	9	10
21	1	0	1	DX2	11	10
22	1	0	1	$\overline{\text{DX2}}$	10	11
23	1	DX2	$\overline{\text{DX2}}$	$\overline{\text{DX2}}$	12	11
24	1	$\overline{\text{DX2}}$	DX2	DX2	11	12
25	1	1	0	DX2	13	12
26	1	1	0	$\overline{\text{DX2}}$	12	13
27	1	1	DX2	$\overline{\text{DX2}}$	14	13
28	1	1	$\overline{\text{DX2}}$	DX2	13	14
29	1	1	1	DX2	15	14
30	1	1	1	$\overline{\text{DX2}}$	14	15
31	1	1	1	1	15	15

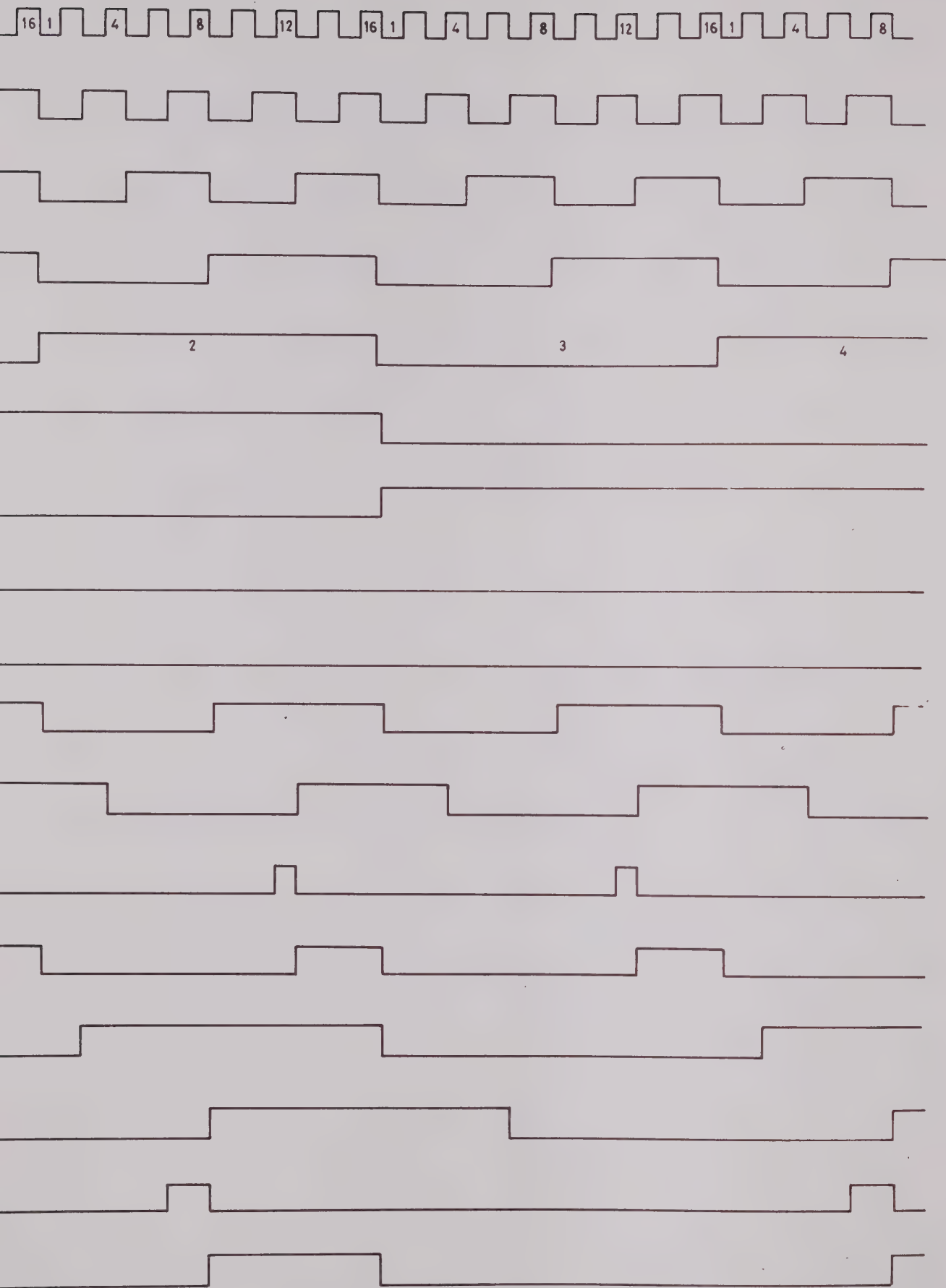


DISPLAY CONTROL 1 FIG 6-7.1





DISPLAY CONTROL 1 PART B TIMING WAVEFORMS FIG. 6-7-3



DISPLAY CONTROL 1 PART C TIMING WAVEFORMS FIG. 6.7.4

DISPLAY CONTROL 2

CHAPTER 6.8

Introduction

Together with Display Control 1, this board provides the waveforms required for the display of alphanumeric characters on the Display Monitor. The Display can accommodate up to 512 characters in a matrix of 32 columns by 16 rows. The area allocated to each character (character cell) is 10 dots wide by 16 dots (rows) high. Normally the character uses only the first nine rows of the character cell, but for lower-case characters with hangers (e.g. p), the first three rows are not used but the following nine are. The Display may also show double-height characters. The character cell is then doubled to 32 rows, and legibility is improved by the application of character rounding.

Display Control 2 contains storage for one complete line of character data, the logic which organises the transfer of data into that store, and the circuits which generate the character video patterns appropriate to the character data. A functional block diagram of the board is shown in fig. 6.8.4.

OPERATION

Loading a Data Line

At the end of t.v. line 12 of each character line, LSL (LINE STORE LOAD) from Display Control 1 becomes high for the remainder of the character line, causing the D.M.A. (Direct Memory Access) Handshake Logic to generate RFRQ (REFRESH REQUEST). On acceptance of the request, the Processor and Cursor Control Board makes RFACK (REFRESH ACKNOWLEDGE) low for a short period (fig. 6.8.3), the Handshake Logic responding to this input by terminating the request and by outputting STR/1 (STROBE/1) to the Character Block Counter. During the period when valid data appears on DAT0 to DAT6 (DATA0-6) and CB (CURSOR BIT), the Processor and Cursor Control Board returns RFACK high. This loads the data (the ASCII code for the first character of the next character line) and the accompanying cursor information into the Input Data Latch, and enables the D.M.A. Handshake Logic to generate another RFRQ signal to request read out of the code for the next character.

The STR/1 pulse clocks the Character Block Counter, which thus keeps a count of the number of characters transferred; also, via the Load Strobe Generating Logic, it generates two (x1) or four (x2) LRC (LINE REGISTER CLOCK) pulses, which load the contents of the Input Data Latch into the Recirculating Line Store via the Cursor Code Generator. Thus after a line of data has been loaded, each x1 character appears twice in the Recirculating Line Store, while each x2 character appears four times.

When 32 characters have been transferred, or when LSL returns low, generation of the RFRQ signal is inhibited.

During the loading of a data line, the Data Selector passes the character data from the Input Data Latch to the Control Code Detector

to enable the x2 and DC1 to DC4 control characters to be detected. When such a character is found, the operation of the Cursor Code Generator is inhibited, thus preventing the character from being loaded into the Recirculating Line Store (see Control Characters).

Video Character Data

The Recirculating Line Store holds the characters (in ASCII format) for one line of data in the required sequence. If these characters are normal height (x1), each one is repeated once (i.e. each character occurs twice); if a character is a double-height character (x2), it is repeated three times (i.e. it occurs four times). The characters are recirculated by a clock derived from LSC (LINE STORE CLOCK). LSC occurs twice during each character period, and thus at the beginning of, and half-way through, a character period, the character data appropriate to that period passes through the Data Selector to the Character Generator and the Control Code Detector.

For normal characters, ROMEN (ROM ENABLE) is active from the beginning of t.v. line 1 to the end of t.v. line 9; for lower-case characters with hangers (e.g. p), ROMEN is active from the beginning of t.v. line 4 to the end of t.v. line 12. RA1 to RA4 (ROW ADDRESS 1 to 4) changes for each t.v. line during the data line. Thus during each character period, the ASCII character code accesses the character video pattern in the Character Generator, while RA1 to RA4 access the required line of that pattern. As an example of this action, the video pattern for an upper case A is shown in fig. 6.8.1A.

As the end of a character period approaches, LDR (LOAD DISPLAYED REFERENCE) loads the line data for the next character from the Character Generator into the Display Data Latch (fig. 6.8.2). At the end of the period, LDD (LOAD DISPLAYED DISPLAY) loads the line data into the Display Register from the Display Data Latch and into the Reference Register from the Character Generator. (The Reference Register, Pre-Rounding Logic and Post-Rounding Logic are only effective when double-height characters are in use). Under the control of CK*, the seven bits of line data are then fed serially from the Display and Reference Registers to the Video Driver.

Character Rounding (fig. 6.8.5)

Outline of Principles. When a double-height character is to be displayed, many of the control waveforms operate at half the normal frequency. This results in the character generating a video pattern which is four times the area of a normal video pattern. Thus at the character generator output, the video pattern for a double-height, upper-case A appears as shown in fig. 6.8.1B.

The column bits are now twice the period of those of normal characters, and the row data is repeated for each row. If this pattern were displayed, a somewhat 'stepped' character would appear. If, however, half-column bits could be added to the pattern where the steps occur, a more rounded and legible character could be produced, as shown in fig. 6.8.1C. This insertion of half-column bits is termed 'character rounding'.

Character rounding operates by comparing the dot information (column bit) in two consecutive lines. To enable this, the row data is sent to

the display twice. The first time it is sent, it is compared with the data sent to the display for the previous row. The second time it is sent, it is compared with the data that will be sent for the next row. When the comparison detects two dots in a diagonal relationship anywhere in the video pattern, it interprets this as an attempt at a diagonal line and inserts a half-column bit at the point required to complete the diagonal. Consider the case of row address 2 of fig. 6.8.1B. The first time that the row data is sent to the display:

- (a) A post-rounding half-column bit is added in the first half of column bit 04 (fig. 6.8.1C), because column bit 03 forms a diagonal with column bit 04 of the previous row.
- (b) A pre-rounding half-column bit is added in the second half of column bit 04, because column bit 05 also forms a diagonal with column bit 04 of the previous row.

The second time that column bit 04 is sent to the display:

- (c) A pre-rounding half-column bit is added in the second half of column bit 02, because column bit 03 will form a diagonal with column bit 02 of the next row.
- (d) A post-rounding half-column bit is added in the first half of column bit 06, because column bit 05 will form a diagonal with column bit 06 of the next row.

Operation. The row data to be displayed is loaded into the Display Data Latch from the Character Generator by LDR. The row address is now changed to that of the previous row. LDD then loads the Display Register with the current row data from the Display Data Latch and the Reference Register with the previous row data from the Character Generator. When the next t.v. line occurs and the row data is loaded into the Display Data Latch a second time, the row address changes from that of the current row to that of the next row. LDD then again loads the Display Register with current row data, but loads the Reference Register with the data for the next row. The relationship between the 32 t.v. lines forming a double-height character, the display row address and the reference row address is shown in table 7.2, Chapter 6.7.

The outputs of the Display and Reference Registers are compared by the Pre-rounding Detector and the Post-rounding Detector. The data is clocked serially through the two registers by CK*. The column bit to be displayed appears at QG of the Display Register, with QH giving the previous bit and QF the next bit. If QG of the Display Register goes low, the Detectors are bypassed and a low appears at IC2A/6 for a full column-bit period. This is inverted to cause a bright-up on the display screen. If QG of the Display Register is high and QG of the Reference Register is low, then the conditions for the insertion of a half-column bit are:

- (a) Pre-rounding - QF of Display Register low, QF of Reference Register high.
- (b) Post-rounding - QH of Display Register low, QH of Reference Register high.

With the preceding conditions for the generation of full and half-column bits, the outputs appearing at IC2A/6 are as shown in fig. 6.8.2.

Video Output

The character video pattern and the FB (FRAME BLANKING), LB (LINE BLANKING) and GRAPHIC VIDEO signals are Or'ed together and the resultant passed to TR2 in the Video Driver. The amplitude of this data is dependent on the condition of bistable IC6A/9. The bistable is set if a high appears in the m.s. bit of the recirculating store output, causing the displayed character to appear dimmer than the other characters; the facility is controlled by control characters DC1 to DC4 (see below). The amplitude of the SYNCs waveform is independent of the control characters.

Control Characters

While data is being loaded for a line of characters, the Control Code Detector examines the data for DISPLAY CONTROL characters DC1 to DC4, and for the x2 control character.

Control characters DC1 to DC4 define the video attributes as follows.

Control Character	Video Intensity	State
DC1	Bright	Steady
DC2	Bright	Flashing
DC3	Dim	Steady
DC4	Dim	Flashing

The detection of any one of the characters clears bistable IC6A/5 to generate CCI (CONTROL CHARACTER INHIBIT). This prevents the character from being passed through the Cursor Code Generator and thus from being loaded into the Recirculating Line Store.

Characters DC1 and DC2 set bistable IC6B/3, and on transfer of the next character (the one which is to be brightly displayed) bistable IC8B/3 sets to make DVL (DATA VIDEO LEVEL) low. This sets the m.s.b. of the Cursor Code Generator low, and this, together with the character to be brightened, is then loaded into the Recirculating Line Store.

Characters DC2 and DC3 set bistable IC6B/5, and on transfer of the next character (the one required to flash) bistable IC8B/5 sets to generate BB (BLINK BIT). The latter is Anded with BL2 (BLINK LEVEL 2), which is FB divided by 32. Thus some frames of data will have the character which is to flash inhibited (by a similar action to that of CCI) while some will not, and this will cause the character to flash.

Gate IC5B/10 detects when a double-height character is required. Signal Cx2 causes bistable IC12C/9 to set as the x2 character is transferred. Bistable IC12D/9 immediately sets to generate x2 MODE. When the Character Block Counter reaches a count of 36, IC12D/5 is set and generates x2 via IC14C/3. When LSL returns low at the end of t.v. line 16, IC12C/9 and IC12D/9 are cleared and x2 MODE returns low. After a line of double-height characters has been displayed, LSL* goes high, the positive edge which thus occurs clearing IC12D/5 to return x2 low.

While the characters are being read out of the Recirculating Line Store for display, the Control Code Detector looks for lower-case characters with hangers (e.g. p), Cursor characters and Null characters. The circuit elements used to detect these characters are as follows.

Character	Gate
Null	IC4A/1
Cursor	IC4A/4
P	IC4C/13
y	IC4C/1
q	IC4C/4
j	IC5B/13
g	IC4D/10

The detection of one of the lower-case characters causes the generation of SHIFT, which alters the row address (see Control Display 1). The detection of a Cursor or a Null character results in the Character Generator being disabled, so that no video pattern from that source is displayed. The detection of a Cursor character also causes the Display and Reference Registers to be loaded with highs, resulting in a blank being presented initially on the display screen. However, when the twelfth t.v. line occurs, L12* generates CB (CURSOR BIT) via IC5A/11, clearing the Display and Reference Registers. Thus on t.v. line 12 of the display, the cursor appears as a 7-column bar.

ROW ADDRESS RA 1 to 4	COLUMN BITS						
	01	02	03	04	05	06	07
1	H	H	H	L	H	H	H
2	H	H	L	H	L	H	H
3	H	L	H	H	H	L	H
4	L	H	H	H	H	H	L
5	L	H	H	H	H	H	L
6	L	L	L	L	L	L	L
7	L	H	H	H	H	H	L
8	L	H	H	H	H	H	L
9	L	H	H	H	H	H	L

A. SINGLE HEIGHT CHARACTER

ROW ADDRESS RA 1 to 4	COLUMN BITS						
	01	02	03	04	05	06	07
1	H	H	H	H	H	L	L
2	H	H	H	H	L	L	H
3	H	H	L	L	H	H	H
4	L	L	H	H	H	H	H
5	L	L	H	H	H	H	H
6	L	L	L	L	L	L	L
7	L	L	H	H	H	H	H
8	L	L	H	H	H	H	H
9	L	L	H	H	H	H	H

B. UNROUNDED DOUBLE HEIGHT CHARACTER

NOTE : HALF COLUMN BITS SHOWN CIRCLED

C. ROUNDED DOUBLE HEIGHT CHARACTER

ROW ADDRESS RA 1 to 4	COLUMN BITS						
	01	02	03	04	05	06	07
1	H	H	H	H	L	L	H
2	H	H	H	L	L	L	L
3	H	L	L	L	H	H	L
4	L	L	L	H	H	H	H
5	L	L	H	H	H	H	H
6	L	L	L	L	L	L	L
7	L	L	H	H	H	H	H
8	L	L	H	H	H	H	H
9	L	L	H	H	H	H	H

FIG 6.8.1 CHARACTER VIDEO PATTERNS

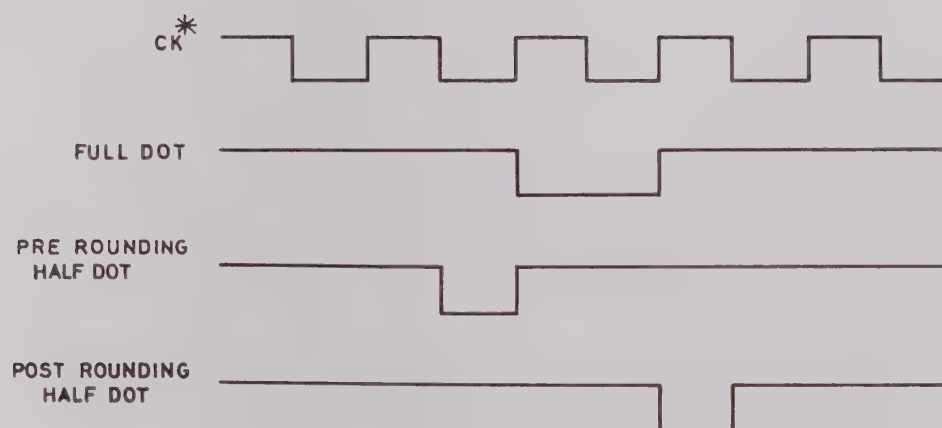
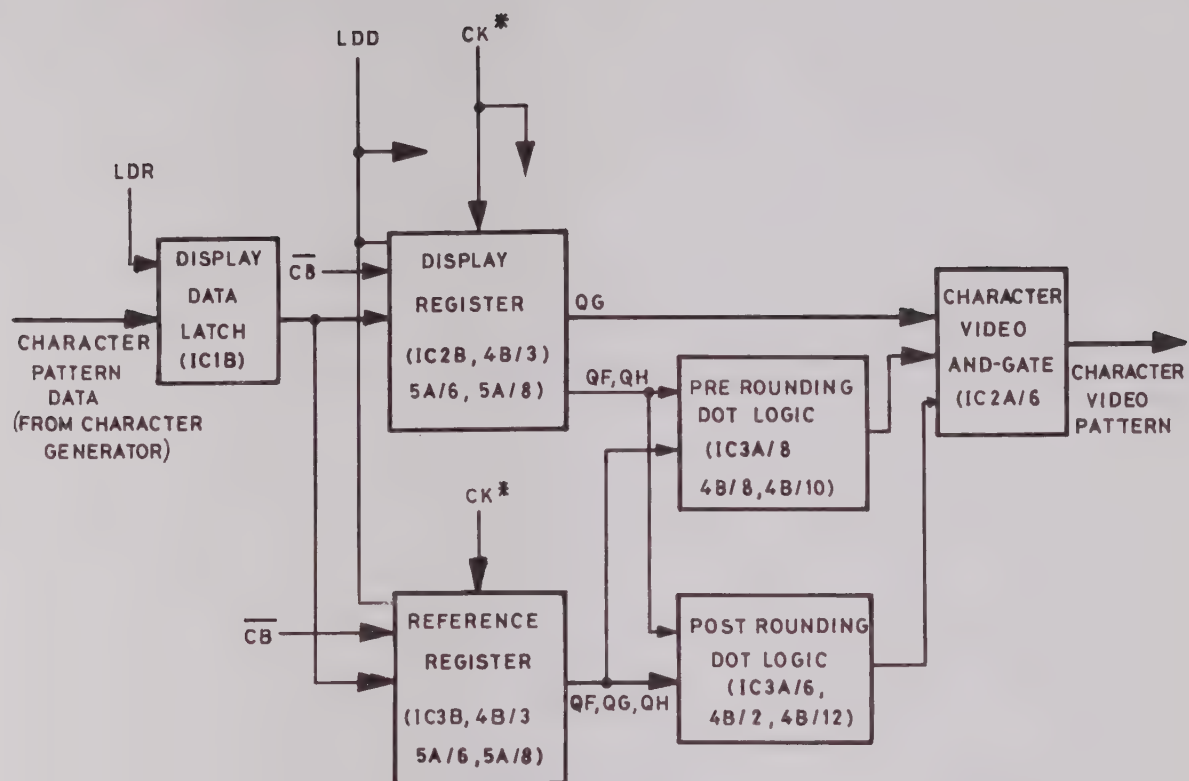
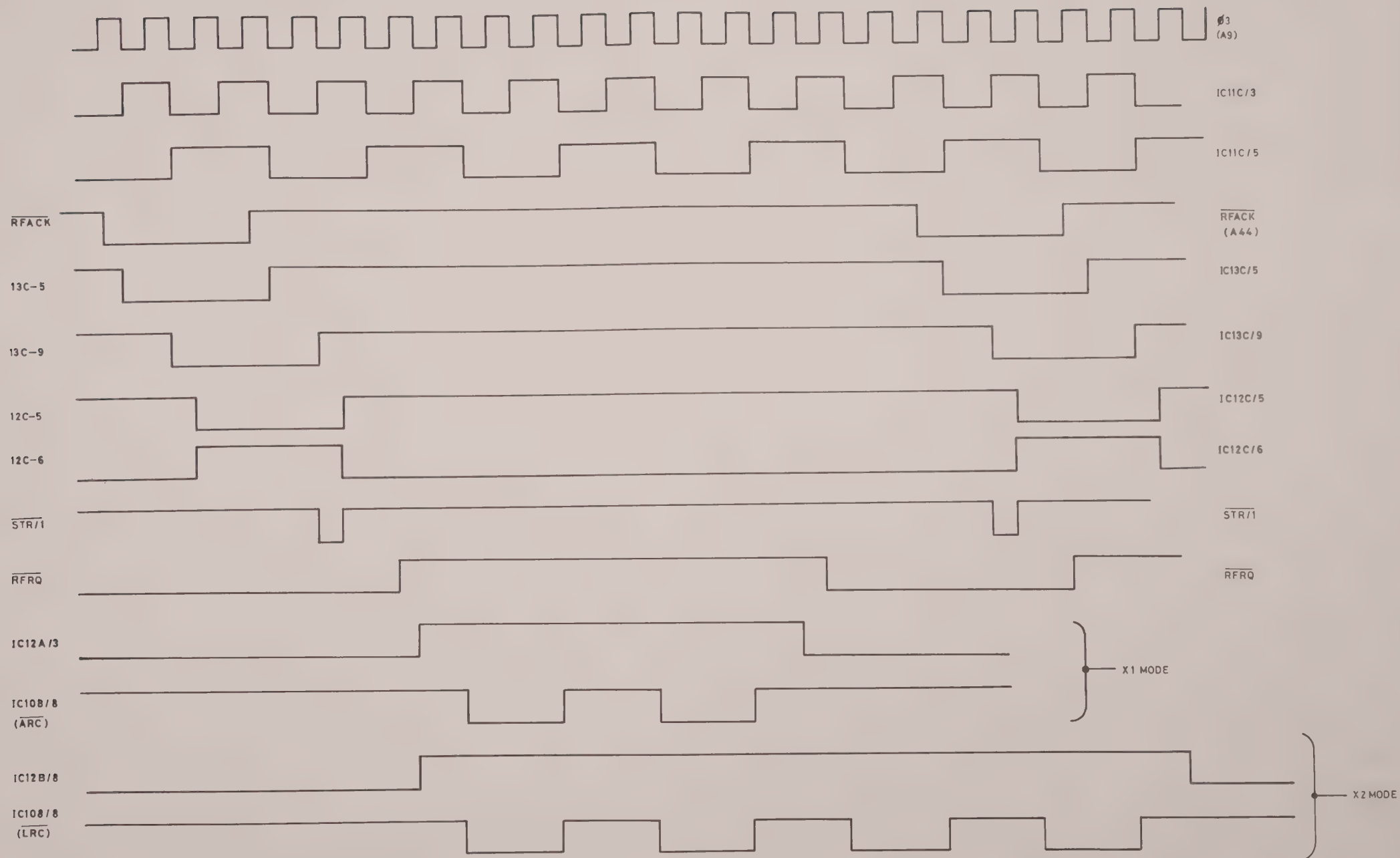
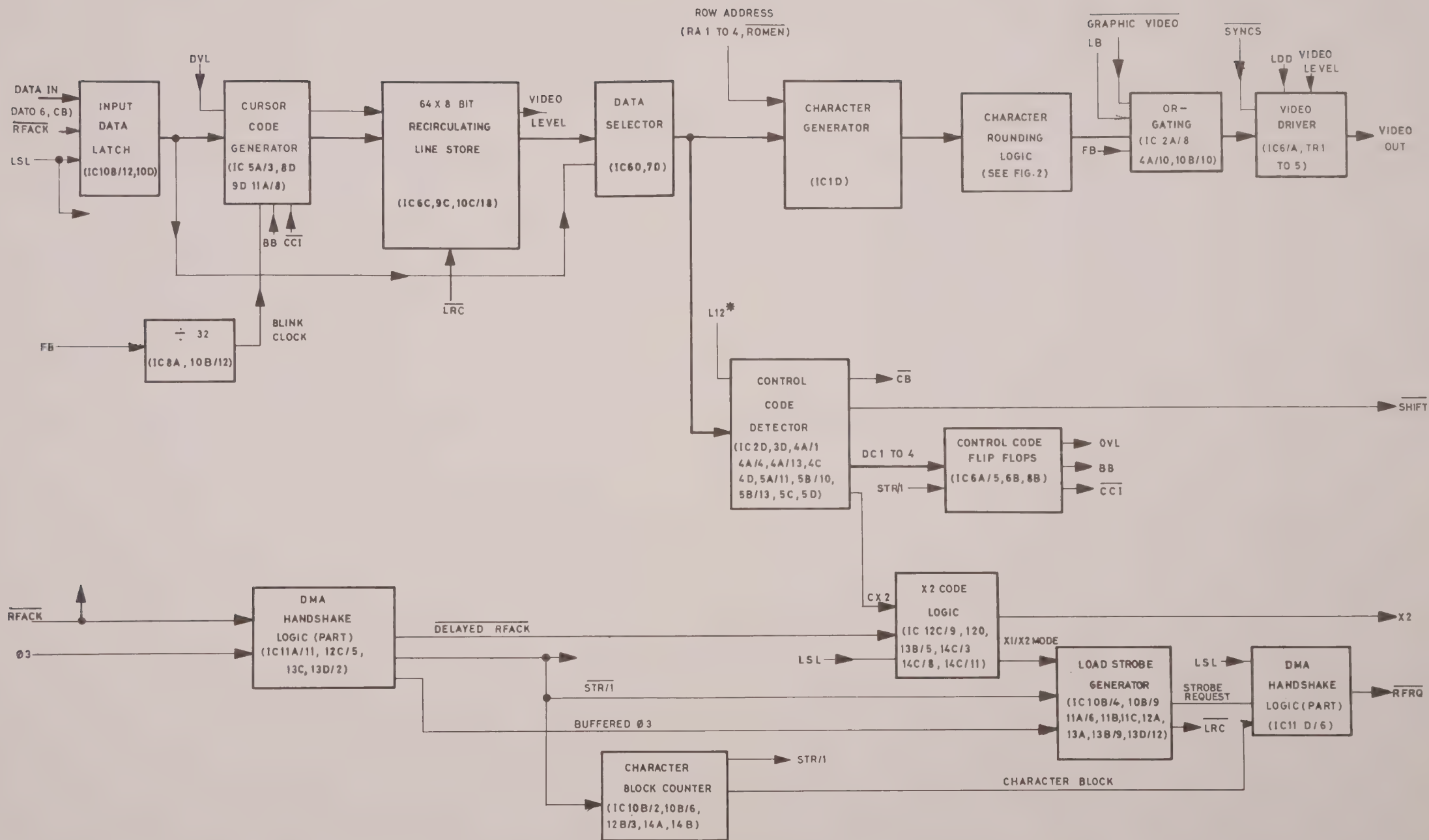


FIG 6.8.2 CHARACTER ROUNDING LOGIC



D.M.A. HANDSHAKE LOGIC TIMING FIG 6.8.3



DISPLAY CONTROL FIG. 6.8.4

ALPHANUMERIC CONTROL BOARD

Introduction

This board provides the waveforms required for the display of alphanumeric characters on the display monitor and the synchronising waveforms required to provide a stable video display. The display can accommodate up to 512 characters in a matrix of 32 columns by 16 rows. The area allocated to each character (character cell) contains 16 TV scan lines, the character using only the first twelve lines. A functional block diagram of the board is shown in Fig 6.8A.1.

Operation

Timing Diagrams. The relative timing of the various waveforms generated by the board circuits is shown in figs 6.8A.2, 6.8A.3 and 6.8A.4 to which reference should be made during the descriptions which follow.

Main Timing Waveform Chain The 6.144 MHz Ø3 system clock feeds a dividing chain the outputs from which are encoded to generate various waveforms. The chain is divided into five stages as shown in Fig 6.8A.1. These are:

- (a) divide-by-10 stage, which provides a character line waveform D to feed,
- (b) divide-by-39 stage, which produces TV line waveform TVA5 to feed,
- (c) divide-by-16 stage, of which the final output, TVA9 has a cycle time equivalent to one data line (a row of characters) and feeds,
- (d) divide-by-18 stage, which gives a frame line waveform, TVA14 or FB (frame blanking),
- (e) divide-by-32 stage fed from FB which generates the blink waveforms BL1 and BL2.

Sync Generator. This logic produces the waveforms described below.

LSL (LINE STORE LOAD). This allows data for one line of characters to pass from the input data latch into the recirculating line store. It is produced by ANDing TVA8 and TVA9 in gate 2B/3, giving a waveform which is high for the last 4 TV lines of a character cell (lines 12-15).

$\overline{\text{LB}}$ (LINE BLANKING).

$\overline{\text{LB}}$ suppresses any video signals at the end of the line period during flyback. It is generated by latch 4A/6. TVA5 is clocked into the latch by E to delay it by one character period, allowing time for the last character to be shifted out of the video shift register.

$\overline{\text{SYNCS}}$.

This signal is a combination of $\overline{\text{SYNC1}}$ and $\overline{\text{SYNC2}}$ (line synchronising pulses) and VS and $\overline{\text{VS}}$ (vertical synchronising pulses). The negative-going edges are extracted by the display monitor circuits for synchronising the oscillator, while the positive $\overline{\text{VS}}$ portion is used by the same oscillator. $\overline{\text{SYNC1}}$ is the inverse of TVA5 $\overline{\text{TVA2}}$ $\overline{\text{TVA1}}$ and $\overline{\text{SYNC2}}$ is TVA1 $\overline{\text{TVA2}}$ $\overline{\text{TVA5}}$. After inversion by 5B/8, the two waveforms combined give a negative-going edge at the beginning of character period 35. The generation of VS is described below.

$\overline{\text{VS}}$ (VERTICAL SYNCHRONISATION). This provides the frame synchronisation for the display monitor in the $\overline{\text{SYNCS}}$ waveform. $\overline{\text{VS}}$ is generated by latch 4B/5 and goes low from the end of data line 16 to partway through data line 17.

$\overline{\text{RR}}$ (RESET REFRESH).

This is used to reset the DMA (refresh) address counter on the processor and cursor control board. It is generated by latch 4A/8. The FB signal is clocked into the latch by TVA10 during character period 18 and cleared by line 11 in the same period to allow DMA to commence on line 12.

Loading a Data Line (Fig 6.8A.4). At the end of TV line 12 of each character line, LSL (LINE STORE LOAD) becomes high for the remainder of the character line, causing the DMA (direct memory access) handshake logic to generate $\overline{\text{RFRQ}}$ (REFRESH ACKNOWLEDGE) low for a short period, the handshake logic responding to this input by terminating the request and by outputting a strobe pulse $\overline{\text{STR/1}}$ to the character block counter. During the period when valid data appears on DAT0 to DAT6 (DATA0-6) and CB (CURSOR BIT), the processor and cursor control board returns $\overline{\text{RFACK}}$ high. This loads the data (the ASCII code for the first character of the next character line) and the accompanying cursor information, into the input data latch, and enables the DMA handshake logic to generate another $\overline{\text{RFRQ}}$ signal to request read out of the code for the next character.

The $\overline{\text{STR/1}}$ pulse clocks the character block counter, which thus keeps a count of the number of characters transferred; and also, via the load strobe generating logic generates a line store input clock pulse, SI, which loads the contents of the input data latch into the recirculating line store via the cursor code generator. When 32 characters have been transferred, or when LSL returns low, the line 0 generation of the $\overline{\text{RFRQ}}$ signal is inhibited.

Line Store. The recirculating line store holds the character codes and video brightness level bits for one row of characters, in the required sequence. The store is a first-in, first-out register (FIFO) IC9D and IC10C capable of holding up to 64 bytes. It is operated by two independent clocks, SI and SO. The output clock SO, derived from (LSL TVA5 D) in gate 11B/12 is used to clock data out of the FIFO at the character rate. The input clock SI, generated in gates 12B/8 clocks data into the FIFO either from the output, when data is required to be recirculated or from the input data latch when new data is being loaded by DMA.

During recirculation, the input clock runs at the character rate, and the input data selector 10D and 11C is switched to recirculate by LSL.

During loading, the input clock runs at the DMA rate, driven from the DMA logic by STR1, and the input data selector is switched by LSL to receive the data from the input data latch 12D.

The FIFO is cleared by a pulse generated from the leading edge of LSL by gate 8B/8. During loading, the output data selector is switched by LSL to receive the incoming data directly, so that the video control codes can be detected and the video brightness level bit generated and fed into the line store along with the character data.

Control Characters. While data is being loaded for a line of characters, the control code detector examines the data for DISPLAY CONTROL characters.

Control characters define the video attributes as follows:

Control Character		Video Intensity	State of Display
OCTAL (HL)	ASCII		
00	NUL	off	blank
01	-	dim	alpha inhibit
21	DC1	bright	steady
22	DC2	bright	flashing
23	DC3	dim	steady
24	DC4	dim	flashing

The detection of any one of the DC characters clears bistable 7A/5 to generate CCI (CONTROL CHARACTER INHIBIT). This prevents the control character from being passed through the cursor code generator and thus from being loaded into the recirculating line store.

Characters DC1 and DC2 set bistable 10A/5, and on transfer of the next character (the one which is to be brightly displayed) bistable 10A/3 sets to make DVL (DATA VIDEO LEVEL) low. This sets the m.s.b. of the cursor code generator low, and this, together with the character to be brightened, is then loaded into the recirculating line store.

Characters DC2 and DC3 set bistable 8A/3, and on transfer of the next character (the one required to flash) bistable IC8A/5 sets to generate BB (BLINK BIT). The latter is ANDed with BL2 (BLINK LEVEL 2), which is FB divided by 32. Thus some frames of data have the character which is to flash inhibited (by a similar action to that of CCI) while some do not, and this causes the character to flash.

The NUL character, when detected by gate 6A/4, clears the video shift register by setting 6B/6 low and inhibits the LOAD signal by turning off gate 6B/3. The video shift register goes on shifting out a series of zeroes, resulting in a blank display so long as NUL is true.

NUL is generated either by sending a NUL from the system data bus, or as a result of the CCI signal turning off the cursor code selector.

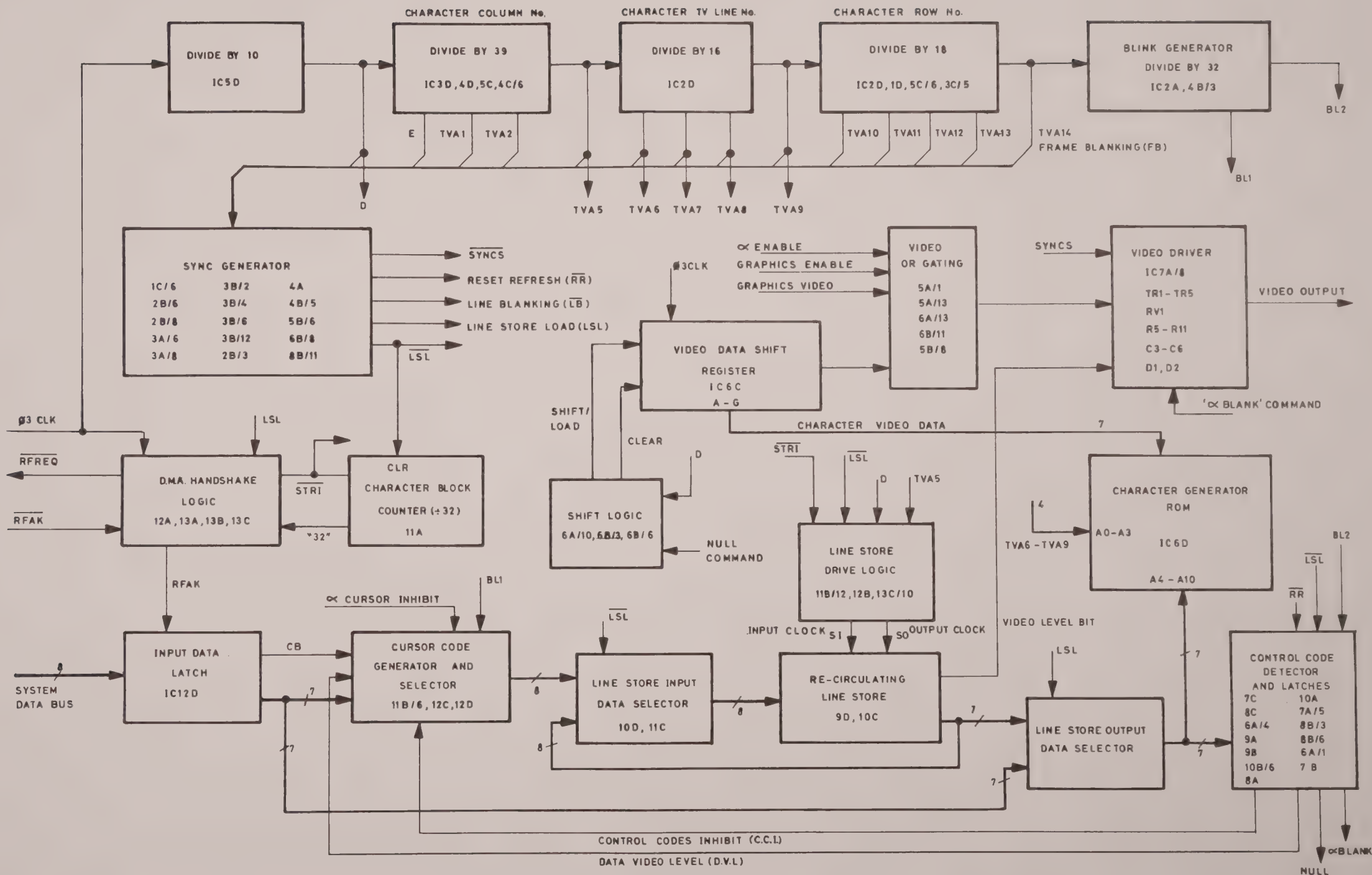
The ALPHA INHIBIT code is described in 2.7 Video Output (below).

Video Output. The line blanking LB and frame blanking FB signals are combined in OR gate 6B/11 and switch TR2 in the video output stage. The SYNCs waveform switches TR4. The alphanumeric video signal from 6C/13 is combined with the graphics video signal from the graphics control board in gates 5B/8 and also switch TR2. When the graphics option is not fitted LINK 1 disables the graphic input and the ENABLE input is open circuit, permanently enabling the alphanumeric video signal.

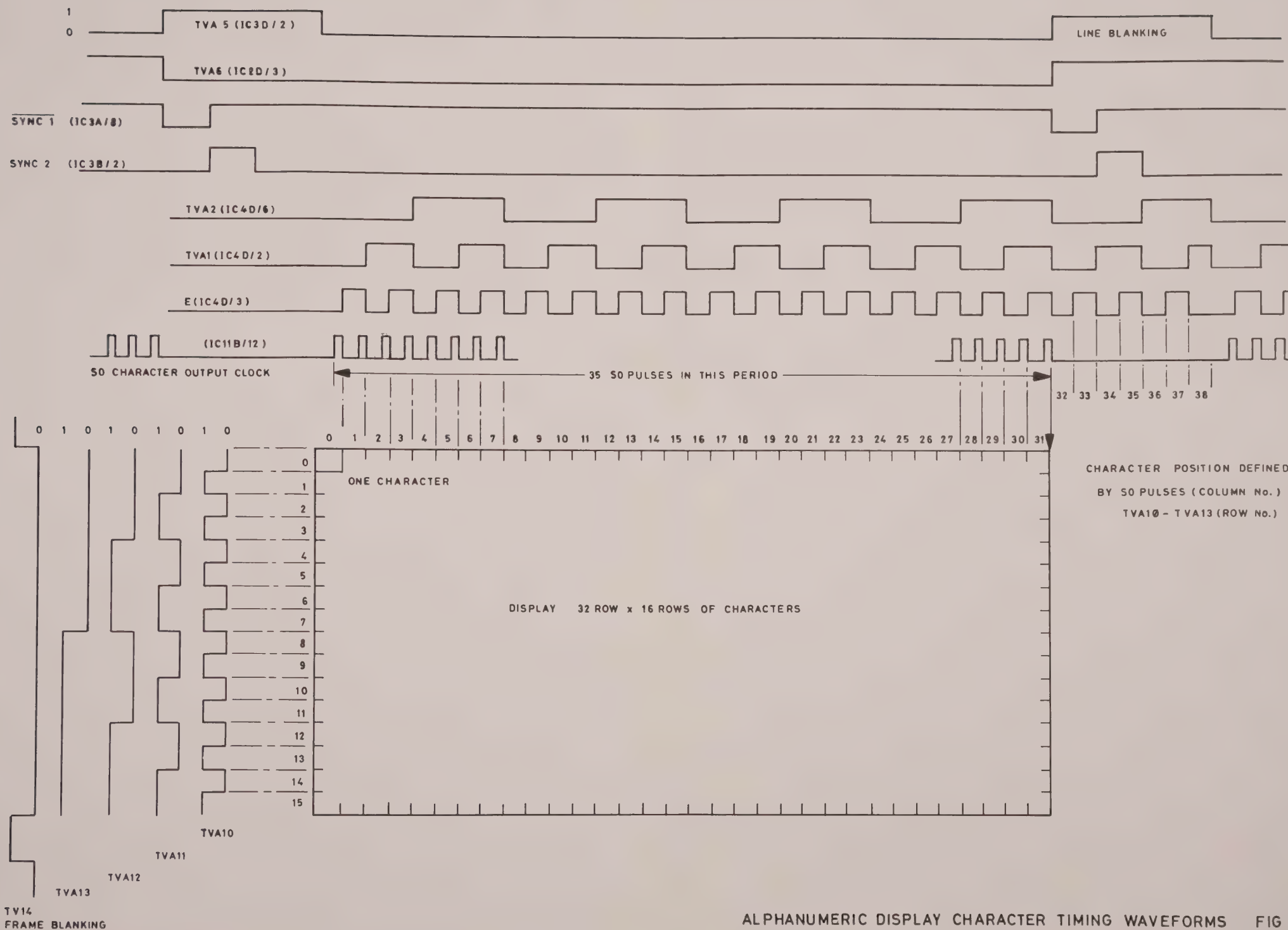
The video brightness level is controlled by the current level in TR1, set up by RV1, and switched bright or dim by the output of latch 7A/8. This latch is clocked at the character rate by D, the output level depending on the state of the video level bit from the line store for that character.

The latch can be held reset by a control character, decoded by gates 6A/1 and 7B/8. This sets latch 7B/3, holding 7A/8 reset blanking off the alphanumeric signal for the remainder of that frame until cancelled by RESET REFRESH.

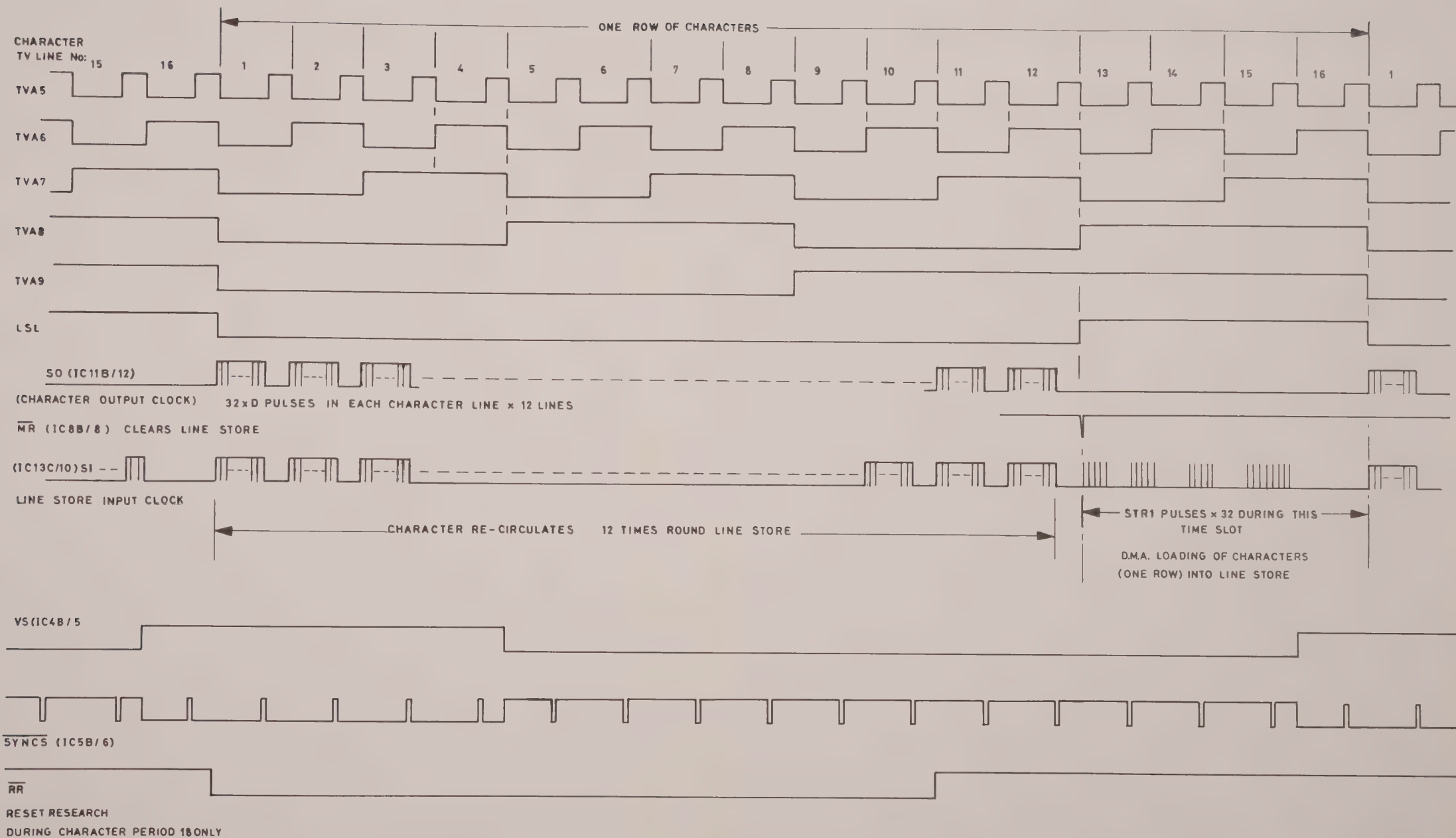
Cursor Generation. The CURSOR BIT (CB) from the input data latch, is fed through gate 11B/6, where, so long as the ALPHA CURSOR ENABLE signal is present, it is switched on and off by the BLINK signal BL1 from the blink generator 11A/6. The output waveform from this gate operates on the cursor code selector, 11D and 12C, alternatively switching the character input data or the cursor character through to the line store. The cursor character is generated by wiring the cursor inputs of the selector to a pre-set pattern which is decoded by the character generator ROM 6D to produce the cursor display.



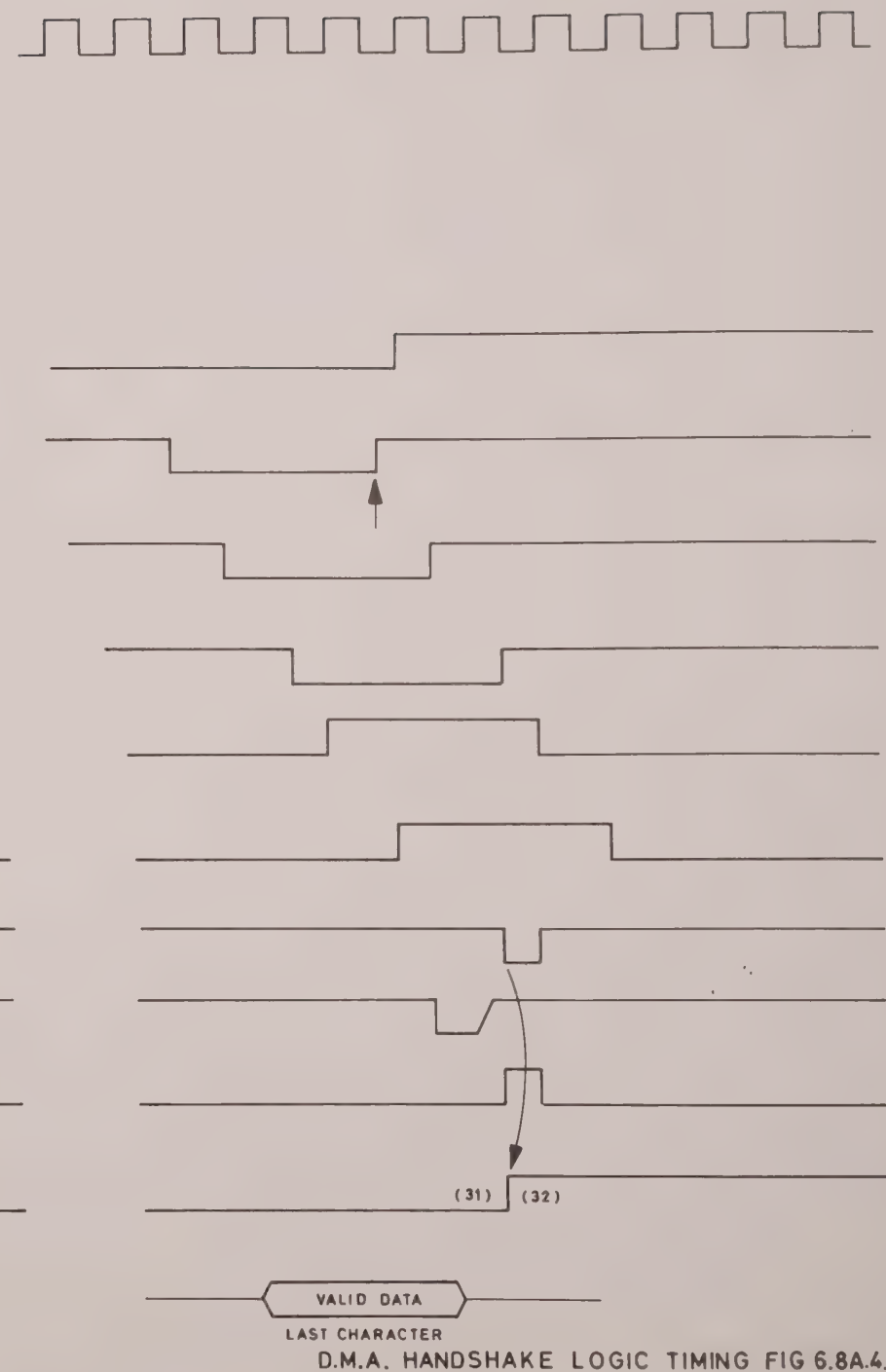
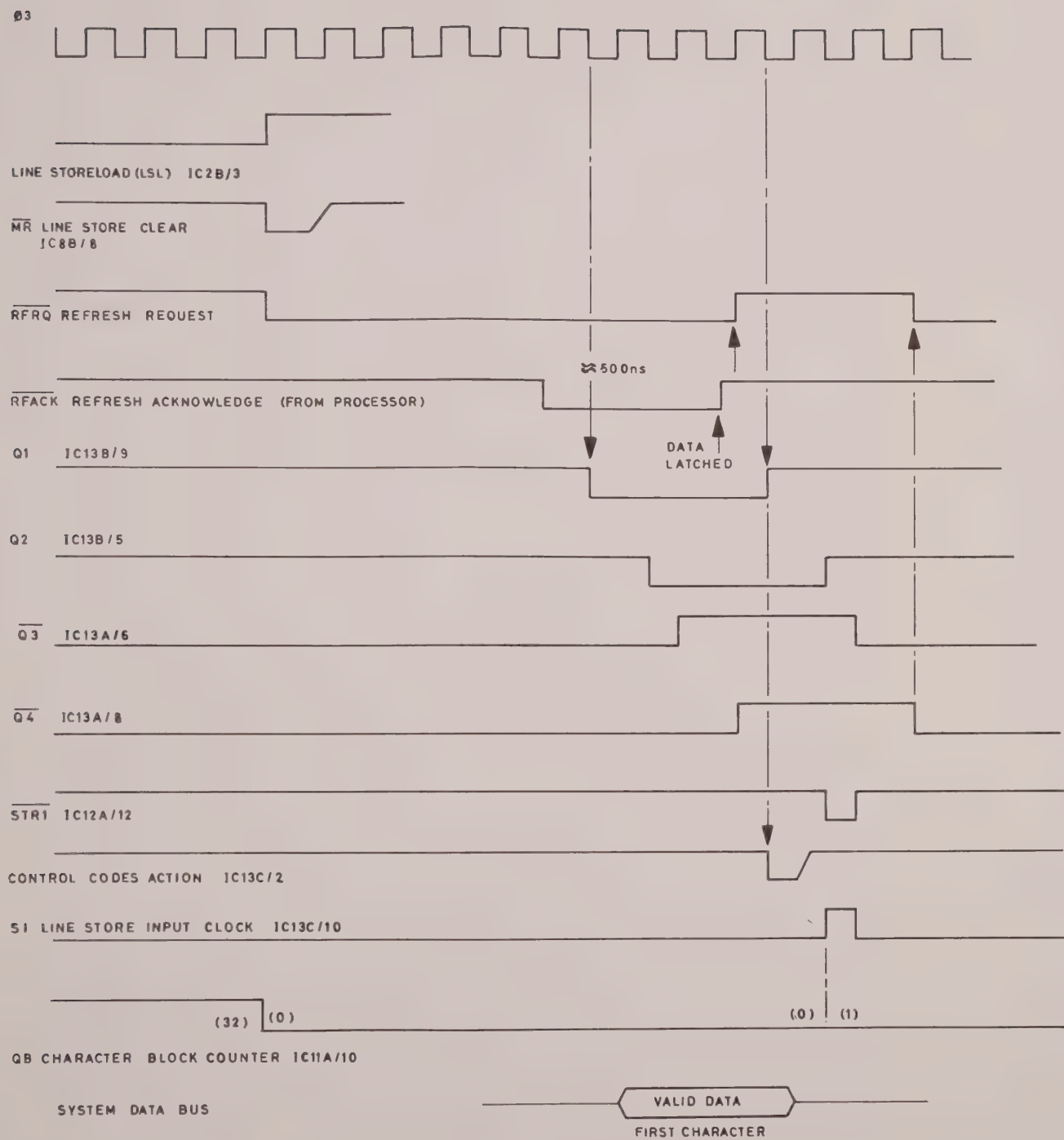
ALPHANUMERIC DISPLAY CONTROL FIG 6.8A-1



ALPHANUMERIC DISPLAY CHARACTER TIMING WAVEFORMS FIG 6.8A.2.



ALPHANUMERIC DISPLAY TIMING WAVEFORMS FIG 6.8A.3.



D.M.A. HANDSHAKE LOGIC TIMING FIG 6.8A.4.

Introduction

The Display Monitor is a conventional, general-purpose data display requiring only the connection of the appropriate primary power supply lines and input signal to enable its operation. The unit is largely modular in construction, and hence the description which follows is restricted to outlining the principal features of the circuit.

A circuit diagram of the monitor is shown in section 8.

OPERATION

Input Signal

The input signal applied to the circuit is a composite signal, formed at the Display Control Board 2 by combining the video signal and the mixed line and field synchronising signals. The input socket presents a 75-ohm termination to the source.

Video Amplifier

The Video Amplifier drives the c.r.t. cathode, and also passes a low-level output to the Line and Field Processor for synchronisation purposes. The module has a bandwidth of 10 MHz and a nominal gain of 37 dB. The signal passed to the tube has its most positive excursion (usually the sync. pulse tip) restored to the quiescent level of the video output stage.

Line and Field Processor

The Line and Field Processor extracts the synchronising signals from the composite signal and supplies corresponding line and field drive signals to their respective deflection output stages. External, preset line and field hold controls are provided.

Field Deflection

Preset height and linearity controls are fitted in the Field Amplifier circuit, enabling the operational differences between individual tubes to be accommodated.

Line Deflection

The Line Amplifier provides the line amplification and output functions. The width control provides sufficient variation of picture width to enable any tube of the approved type to be used, and S correction is included in the circuit. The retrace time is 8 μ s, which permits the use of most character systems.

Scan Coils

The Scan Coils assembly consists of a short ferrite ring carrying a saddle-wound line coil and a toroidal-wound field coil; shift rings

and a neck clamp are included. To reduce raster distortion, picture-shape-correction magnets can be mounted on the pegs provided around the periphery of the plastic moulding containing the assembly. A linearity sleeve is fitted over the c.r.t. neck inside the scan coils.

Flashover Protection Board

In accordance with normal c.r.t. practice, all connections to the tube electrodes other than the anode 2, anode 4 and heater connections are made via resistive decoupling; also, a protective spark gap is fitted at each of these electrodes and at each side of the heater.

Power Supplies

The +12V primary supply required by the monitor is connected from the system +12V bus, together with the associated 0V line. An l.e.d. provides a 'power on/failed' indication.

The line transformer (T1) provides 12 kV e.h.t. to the tube via the e.h.t. rectifier. The tube heater supply (11.3V approx.) is obtained from the +12V primary supply via D6. All other d.c. supplies required by the monitor circuits are developed within the monitor, utilising the auxiliary outputs from the line transformer.

KEYBOARD

CHAPTER 6.10

Introduction

The function of the Keyboard is to provide the F.R.A. with a man-machine interface via which the operator can enter commands and data (see section 4). A functional block diagram of the unit is given in fig. 6.10.1.

OPERATION

Keyswitch Matrix Scanning

Under the control of the 400 Hz clock input, the Scanner continually generates sequential, 7-bit, binary output codes ($\overline{A0}$ to $\overline{A7}$, where $\overline{A0}$ is the l.s.b.) which enable a keyswitch matrix of up to 128 stations to be interrogated on a station-by-station basis. The code changes on the falling edge of the clock and thus each code defines a 2.5 μ s 'window' during which a specific key-switch is interrogated and the results of the interrogation processed. The four l.s.b. of the codes are used to scan the matrix columns, and the three m.s.b. to scan the matrix rows.

In the present application, only sufficient codes to sequentially scan an 8 x 5 (40 station) matrix are required. These are obtained by binary-to-decimal decoding the X and Y scan bits in such a manner as to prevent the unwanted codes from being applied to the matrix inputs.

Keyswitch Output Processing

At the start of each 2.5 μ s window, the Keyswitch Detect and Latch circuit is in the reset condition. If at the time it is interrogated a keyswitch is in the operated state, or if it assumes that state during the interrogation, the state is detected and stored by the Keyswitch Detect and Latch circuit, which then signals the fact (SRI) to the Scanner. At the end of each window, the circuit is cleared by the $\overline{\text{RESET}}$ output from the Scanner.

Each SRI input to the Scanner causes that element to encode and output a 6-bit signal which specifies the keyswitch that caused the input, and which is used to address the ASCII Lookup Table. This Table is a 64-word x 7-bit PROM which is programmed to supply the ASCII codes allocated to the characters and functions contained in the keypad. Thus the code appropriate to the operated keyswitch appears at the PA0 to PA7 (Port A0 to 7) inputs of the P.P.I. (Programmable Peripheral Interface). The subsequent STROBE pulse from the Scanner then loads the ASCII code, together with its hard-wired parity bit (PA7), into the P.P.I.

Interfacing

The Vector Address Comparator constantly monitors the System Address Bus bits $\overline{\text{ADD2}}$ to $\overline{\text{ADD7}}$. When the value of these address bits equals the value set in at the Address Selector switch array - i.e. when

the address on the bus is within the range of vector and port addresses allocated to the Keyboard (58 Hex. to 5B Hex.) - the Comparator makes the $\overline{CS}$ (CHIP SELECT) input to the P.P.I. low. This enables communication between the P.P.I. and the System Data Bus; whether this communication takes the form of a Read or a Write operation, and which of the P.P.I. facilities is involved, depends upon the states of the $\overline{IORM}$ (INPUT OUTPUT READ MAPPED) and $\overline{IOWM}$ (INPUT OUTPUT WRITE MAPPED) control signals and of address bits $\overline{ADD0}$ and $\overline{ADD1}$, as described below.

- (a) $\overline{IORM} = \text{low}$, $\overline{IOWM} = \text{high}$, $\overline{ADD0} = \text{low}$, $\overline{ADD1} = \text{low}$: This combination commands a Keyboard Data Register Read, during which the contents of Port A (an ASCII code) are output onto the System Data Bus.
- (b) $\overline{IORM} = \text{low}$, $\overline{IOWM} = \text{high}$, $\overline{ADD0} = \text{low}$, $\overline{ADD1} = \text{high}$: This input configuration is used to command a Keyboard Status Register Read, which places the contents of Port C on the System Data Bus. The functions signalled in the Status Word are as follows:

PC0	Used to disable interrupts during reset.
PC1-PC2	Not used.
PC3	When high, indicates that a keyswitch has been operated, that Port A contains valid data, and that an interrupt has been requested (cannot be set if interrupts are disabled). Reset by reading Port A.
PC4	When low, loads data into Port A.
PC5	When high, indicates that a keyswitch has been operated and that data has been loaded into Port A. The bit is not dependent upon interrupts being enabled. (Not used in the present application).
PC6,7	Not used.

- (c) $\overline{IORM} = \text{high}$, $\overline{IOWM} = \text{low}$, $\overline{ADD0} = \text{high}$, $\overline{ADD1} = \text{high}$: In response to these inputs, a Keyboard Control Register Write operation is performed, during which the contents of the System Data Bus are written to the internal control register.

The Control Word input in this manner can be used for either of two purposes - to define the P.P.I. operating mode or to set and reset bits of Port C. In either case, bits 0 to 6 contain the information necessary for the performance of the control action, while bit 7 is a flag which indicates which of the two actions is required; the format of bits 0 to 6 for both actions is detailed in the manufacturers documentation for the P.P.I. (see chapter 6.1).

In the present application, the mode set action is normally used only for initialising the P.P.I. to Mode 1 following the power-on reset; the bit set/reset action is used to

enable/disable interrupts as required by program.

Interrupts

Providing that interrupts are enabled and the $\overline{\text{STB}}$ input has caused data to be loaded into Port A, then on the rising edge of $\overline{\text{STB}}$, PC3 becomes high to request an interrupt. As in the present P.P.I. configuration PC0 is held low, this results in one of $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$ (INTERRUPT REQUEST 0 to 7), as selected by the Interrupt Request Selector switch array, becoming low to request a microprocessor interrupt.

Power-On Reset

Following the application of power to the F.R.A., the P.P.I. is reset by the $\overline{\text{INTL}}$ pulse input from the Processor and Cursor Control Board. This reset clears all the internal registers, including the Keyboard Control Register, and sets Ports A and C to the input mode.

Mains Failure Reset

An additional circuit is provided by IC1E/7 and TR1 to cope with fractional-cycle mains 'dropouts'. The $\overline{\text{RESET}}$ output is applied to pin 60 of all SKT A-side connectors on the FRA motherboard, being used primarily by the processor and cursor control board.

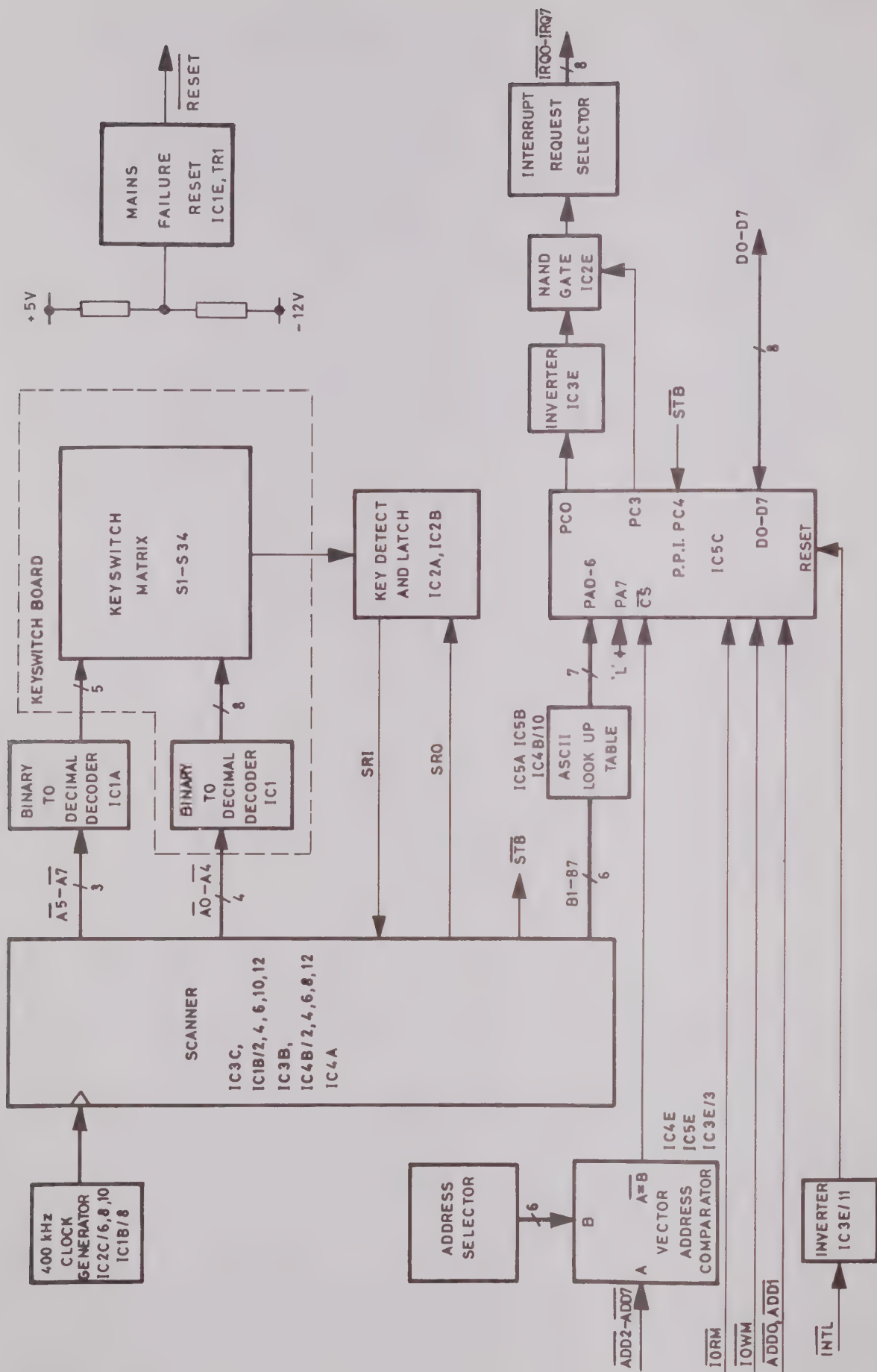


FIG. 6.10.1 KEYBOARD

POWER SUPPLY

CHAPTER 6.11

Introduction

The Power Supply Assembly provides all the d.c. supplies necessary for operation of the Microprocessor, Memory, Generator and Correlator functions together with the primary d.c. supply required by the Display Monitor. The supplies are divided into four groups:

- (a) Group 1 (earthy supplies) - Micro Processor, Memory and Display, Keyboard, Options;

+ 5V 10A (15A fuse)
+12V 2.5A (4A fuse)
-12V 2A

- (b) Group 2 (floating supplies) - Generator; Ext. Sync Board

+ 5V 0.5A
+30V 0.5A
-30V 0.5A

- (c) Group 3 (floating supplies) - Correlator 1,

+ 5V 0.5A
+30V 0.25A
-30V 0.25A

- (d) Group 4 (floating supplies) - Correlator 2;

+ 5V 0.5A
+30V 0.25A
-30V 0.25A

A simplified block diagram of the assembly is shown in fig. 6.11.1 and the circuit diagram in section 8.

OPERATION

Input Circuit

Mains transformer T1 has a split primary winding, the halves of which are connected in parallel by SW2 for an 115V a.c. input, and in series for a 230V input. A 'push to close/push to open' switch SW1, remotely actuated by the MAINS pushbutton on the Display Monitor, connects the mains supply from a connector-filter assembly to SW2 via FS1. The assembly cooling fan is connected across the 115V winding of T1.

Each regulated d.c. supply has an individual, fused T1 secondary winding and full-wave rectifier. Reservoir capacitors are connected across the rectifiers of the higher-rated supplies.

+30V, -30V Supplies - Groups 3 and 4

Since the two supplies are identical in all respects, it is sufficient to describe the Group 3 +30V, -30V control. Paired positive and negative voltage regulators REG7 and REG6 control the base drives of the rail series-pass transistors TR4 and TR3 respectively. Potentiometer RV3 sets the regulator reference level, whilst rail output voltage and balance is determined by the network R12, RV4, R13 and C12, C15 connected between the regulators and the 0V and +30V rails.

Series-pass transistor current-limiting control is derived from the volt drop across rail resistors R11 and R9. Capacitors C16 and C13 connected across the output rails suppress ripple and noise.

+30V, -30V Supplies - Group 2

Control of these 0.5A supplies, with regulators suitable for the rating, is similar to that described in the preceding subsection except that 'fold-back' current limiting is employed. Excessive current demand results in the series-pass transistors TR2 and TR3 being progressively biased back such that, under short-circuit load conditions, the current delivered is reduced to a safe low value.

Consider the -30V rail control. Transistor TR6, connected between the regulator drive (Booster O/P) and Regulated Output terminals, is normally held off by the volt drop across R18. At the limiting turning point the volt drop across current-sensing resistor R20 turns TR6 on, shunting the pass transistor base drive. The load current folds back, reducing to approximately 100 mA under short-circuit conditions, with REG8 drive current increasing to a limiting value set by R10.

With the output tracking network connected between REG8 and REG9 (F/B terminal), +30V control is tracked to that of the -30V supply. Under short-circuit load conditions, the +30V rail current is reduced to approximately 30 mA, set by R30.

Since the rail voltage is only required to be within ± 5 per cent of the nominal value, a potentiometer is not fitted in the output locking network.

+12V, -12V Supplies - Group 1

These two supplies are best considered as isolated rails with +12V (REG11) being set by RV8 and -12V (REG10) by RV6. Protective diodes (D25, D23) are connected across the series-pass transistors TR12 and TR10.

Fold-back current limiting (TR11) similar to that of the Group 2 +30V, -30V supplies is incorporated, RV7 setting the fold-back turning point. Additional resistors R33 and R34 prevent premature fold-back under high capacitive loading. Typically, the +12V short circuit load current is 0.8A with a turning point of 2.8A.

The Group 1 shutdown circuit incorporating opto-coupler OPT1, TR8, TR9, TR13 and TR14 is described under a separate heading.

+5V Switching Regulator Supply - Group 1

A switching waveform of 2:1 mark/space ratio at 30 kHz, generated by oscillator IC1 and applied to REG12 pin 5, controls the series-pass transistor TR15 via gain transistors TR17 and TR16. L1 and L2/C44 provide rail smoothing and spike suppression.

Current limit in this 10A supply, detected by TR20 from the volt drop across R57 and R65, is applied to the F/B terminal of REG12 via inverter TR18.

A crowbar circuit (CSR1) provides high rail voltage fault protection, in particular a pass transistor collector to emitter short circuit. The circuit is gated if the rail voltage exceeds approximately 6V (D33) for longer than the time constant of C38/R62. Overvoltages of shorter duration are clamped by D34.

Remote (load) voltage sensing via PL7 pins 1B and 2B, divided by R58 and R59, is applied to the F/B terminal of the regulator.

Group 1 Fault Shutdown

Provision is made to shutdown the other two supplies should one of the group fail. In each control circuit an f.e.t. switch (TR9, TR13 and TR19) is connected between the low potential rail and the COMP (Shutdown) regulator terminal.

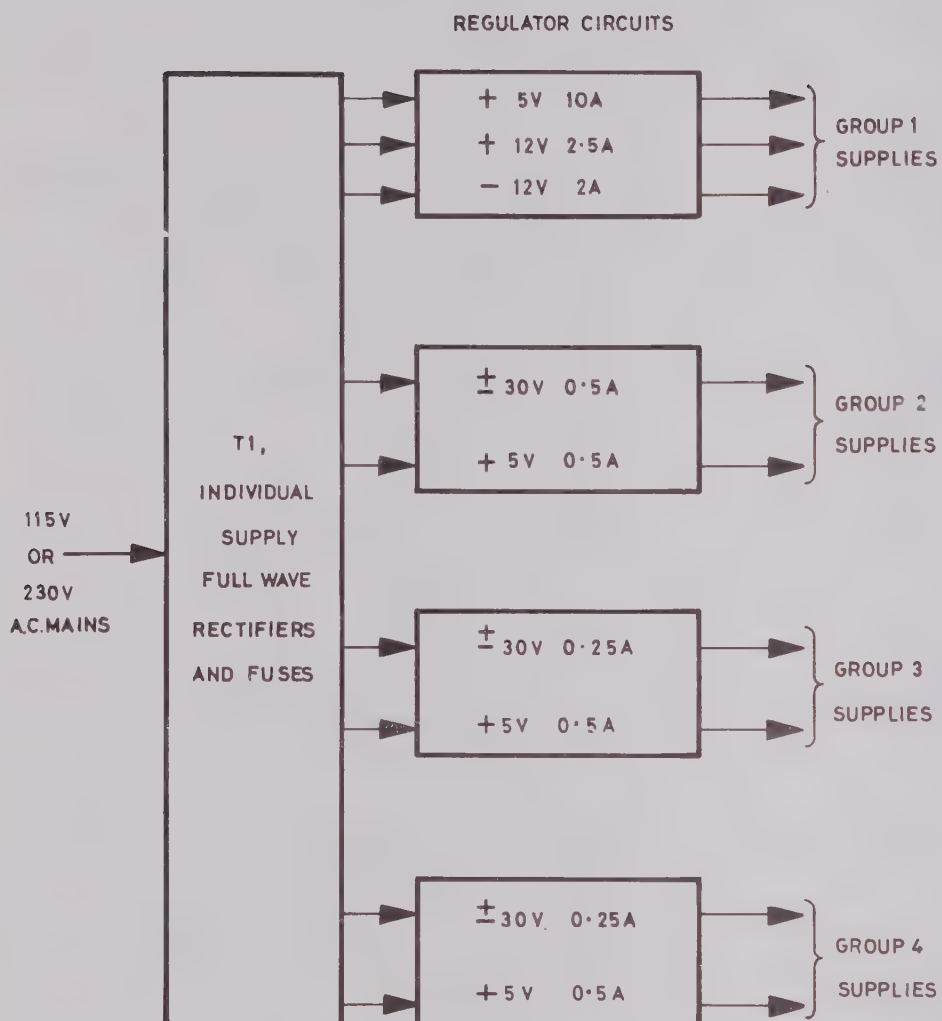
Assume a -12V supply failure. The gates of TR13 and TR19 follow the rail towards zero volts and the f.e.t. turn on, applying zero volts to the COMP (Shutdown) terminals of the +12V and +5V regulators. Both supplies are shut off.

Should the +5V supply fail, or its crowbar circuit operate, f.e.t. TR14 is gated on, short circuiting opto-coupler OPT1, which in turn gates f.e.t. TR9 via TR8. The -12V supply shuts off, followed by the +12V, once a charge has built up on C26. A +12V failure results in f.e.t. TR14 assuming a low impedance state, shutting down the -12V supply followed by the +5V.

Power On Indicators

A 'power on' l.e.d. indicator is fitted on the assembly front panel adjacent to the MAINS pushbutton. This indicator is connected across the +12V and -12V supplies at the Display Monitor motherboard.

An 'output present' l.e.d. indicator is connected across each regulated d.c. supply. The indicators, mounted on the respective p.c.b. or motherboard are visible when the assembly top panel is removed.



POWER SUPPLY ASSEMBLY FIG 6.11.1

SECTION 7

TESTING

Sub-Section	LIST OF CONTENTS	Page No.
1	Introduction	7.1
2	Setting Up the FRA	7.1
3	Test Procedure	7.1
4	Test Box	7.2

1. INTRODUCTION

- 1.1 A test box is provided which can be used to produce a test input to both correlator channels from the generator output. A simple functional test is then performed as below. If the test box is not at hand, a test circuit as shown in sub-section 4 can be substituted.

2. SETTING UP THE FRA

Format	2
Frequency Start	90 Hz
Final	9000 Hz
Gen. Amplitude	5.00 V
Correlator Range	Auto
Channel	B/A
Intervals	11
Co-ordinates	Log-Polar

INTERVAL MODE **LOG**

For all other parameters, default values apply.

3. TEST PROCEDURE

- (a) Plug the test box directly into the input panel on the right hand side of the FRA.
- (b) Press the START and DATA DISPLAY keys. Results should appear as follows:

No.	FREQ Hz	GAIN dB Log R	PHASE °
1	90.00	-20.00	90.00
2	142.6	-16.00	90.00
3	226.0	-12.00	90.00
4	358.2	-8.000	90.00
5	567.8	-4.000	90.00
6	900.0	0.000	90.00
7	1426.	4.000	90.00
8	2260.	8.000	90.00
9	3582.	12.00	90.00
10	5678.	16.00	90.00
11	9000.	20.00	90.00

(c) If the results obtained differ from those shown above by a significant amount, contact your local agent, or:

SE Labs (EMI) Ltd
 Service Dept.
 North Feltham Trading Estate,
 Feltham,
 Middlesex, TW14 OTD
 England.

4. TEST BOX

4.1 Fig 7.1 below is a circuit diagram of the test box. The components used are not high precision and the test box should not be used as a Standard.

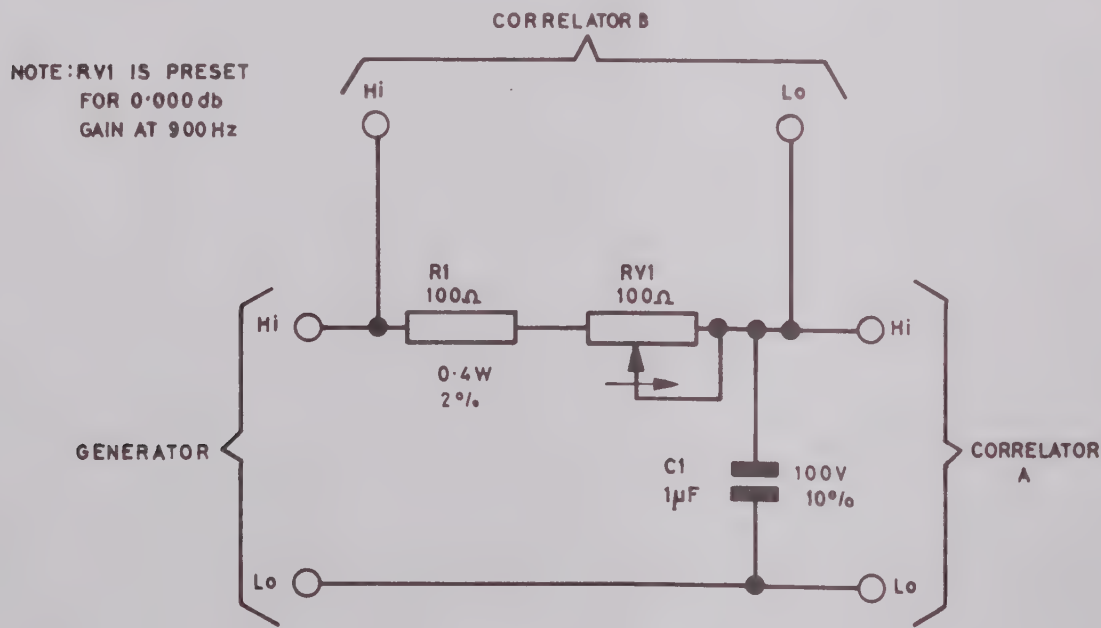


FIG 7.1 TEST BOX CIRCUIT

5. FAULT DIAGNOSIS

The purpose of this procedure is to provide a method of diagnosing faults down to board level.

5.1 Display Checks

- (a) Check that the SE2450 is set for the local mains supply and that the correct value of mains fuse FS1 is fitted.
- (b) Switch on. The LED Indicator should come on.
- (c) The display should appear within 20 seconds; if not, check the adjustment of the BRIGHTNESS and CONTRAST controls behind the keyboard.
- (d) If the display is not steady and synchronised, the LINE HOLD and/or FRAME HOLD potentiometers should be adjusted - see Fig. 4.12 for location of controls, page 4-19. If the raster fails to appear take the following action:
 - (i) Check +12V supply to monitor module
+12V - PL P2-3
0V - PL P2-1
If this is correct, renew monitor module.
 - (ii) If the raster appears but the video is absent, proceed as follows. Using an oscilloscope, check for a composite video signal on the VIDEO OUT SKT on the back panel. If this is present, check the wiring to the monitor module board. If this is correct replace the monitor module board. If the composite video signal is absent, replace display control 2 and/or display control 1, SKT 6 and 7 in the main card frame.

5.2 Keyboard Check

If the keyboard fails to operate:

- (a) Check the address selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	ON	OFF	ON	ON	OFF	OFF

- (b) Check that the interrupt request selector is SET as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF

(c) Check power rails as follows:

PL1-1	+5V	} Group 1
PL1-20	+5V	
PL1-2	0V	
PL1-21	0V	
PL1-3	-12V	

if the checks in steps (a), (b), (c) are correct, renew keyboard.

5.3 Generator Checks

(a) Set Data Entry Form 1 as follows:

Frequency	1000 HZ
Harmonic	1
Gen.amplitude	5.00V r.m.s.
Gen. bias	0V
Correlator range auto	(*)
Channel	A (500V) B (500V)
Integration	(1000) cycles
Delay	(0.5) seconds
Channel	A (*) B () B/A ()
Co-ordinates	Polar

(b) Connect an oscilloscope to the generator O/P sockets and press start. A 1 kHz sinewave with an amplitude of 5.00V rms should be observed. If it is not, proceed as follows:

(i) Connect Generator D/A SKT 13 to an extender board and check that power is present at the following pins:

SKT 13	VOLTAGE	
B14	+30V(F)A	} GROUP 2
B13	+30V(F)A	
B12	0V(F)A	
B11	0V(F)A	
B10	-30V(F)A	
B 9	-30V(F)A	
B 8	+ 5V(F)D	
B 7	+ 5V(F)D	
B 6	0V(F)D	
B 5	0V(F)D	
A 4	0V	} GROUP 1
A 3	0V	
A 2	+ 5V	
A 1	+ 5V	

If these are present renew the Generator D/A board.

- (ii) Connect generator control SKT 12 to an extender board and check that power is present on the following pins:

SKT 12	VOLTAGE	
A 4	0V	GROUP 1
A 3	0V	
A 2	+ 5V	
A 1	+ 5V	
A 5	+12V	

- (iii) Check the address selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF

If these are correct renew the generator control board.

5.4. Correlator Checks

- 5.4.1 Each correlator channel comprises two boards Correlator A/D and Correlator Control. The only difference between Channel A and B in the physical location and the address and interrupt switch settings. By interchanging Correlator A/D, A and B boards and Correlator Control A and B boards it should be possible to identify the faulty board. When only one correlator channel is fitted it must be set up as Channel A.

5.4.2 Channel A

- Link the GENERATOR O/P to CORRELATOR A and B inputs.
Set up DATA ENTRY FORM 1 as detailed in 5.3 Generator Checks.
Press START.
- If an unsatisfactory result is obtained, take the following action:
 - Connect the correlator A/D channel A, SKT 1 to an extender board and check that power is present at the following pins:

SKT 1	VOLTAGE				
B10	+30V	(F)	A	GROUP 4	
B 9	+30V	(F)	A		
B 8	0V	(F)	A		
B 7	0V	(F)	A		
B 6	-30V	(F)	A		
B 5	-30V	(F)	A		
B 4	0V	(F)	D		
B 3	0V	(F)	D		
B 2	+ 5V	(F)	D		
B 1	+ 5V	(F)	D.		
A 4	0V			GROUP 1	
A 3	0V				
A 2	+ 5V				
A 1	+ 5V				

If these are present renew the Correlator A/D board.

- (ii) Check that on Correlator Control Channel A, SKT 2, the address selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	ON	OFF	OFF	ON	OFF	OFF

- (iii) Check that the interrupt request selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF

- (iv) Check that power is present at the following pins:

SKT 2	VOLTAGE				
A 4	0V			GROUP 1	
A 3	0V				
A 2	+5V				
A 1	+5V				

If these are correct, renew the Correlator Control Board.

5.4.3 Channel B

- Select CHANNEL B on DATA ENTRY, FORM 1 and press START.
- If an unsatisfactory result is obtained, proceed as follows:

- (i) Connect the Correlator A/D Channel B, SKT 3 to an extender board and check the following pins:

SKT 3	VOLTAGE	
B10	+30V(F)A	GROUP 3
B 9	+30V(F)A	
B 8	0V(F)A	
B 7	0V(F)A	
B 6	-30V(F)A	
B 5	-30V(F)A	
B 4	0V(F)D	
B 3	0V(F)D	
B 2	+ 5V(F)D	
B 1	+ 5V(F)D	
A 4	0V	GROUP 1
A 3	0V	
A 2	+ 5V	
A 1	+ 5V	

If these are correct renew the Correlator A/D Board.

- (ii) Check that on Correlator Control Channel B, SKT 4, the address selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	ON	ON	OFF	OFF	OFF	OFF

- (ii) Check that the interrupt request selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

If these are correct, renew the Correlator Control Board.

5.5 External Sync Control, SKT 5

- (a) Connect the Ext. Sync. I/P. unit to SKT.39 on the rear panel of the SE 2450 and set up as detailed in External Synchronisation option SE2452 Manual, Section 2. If the unit fails to operate correctly, proceed as follows:

- (b) Check that the power rails to the External Sync. I/P Unit are as follows:

SKT 39	VOLTAGE	
1 and 14	-30V(F)A	GROUP 2
2 and 15	0V(F)A	
12 and 24	+30V(F)A	GROUP 1
13 and 25	+ 5V	
11 and 23	0V	

If these are present, renew the Ext. Sync I/P Unit.

- (c) Check that on the External Sync Control, SKT 5, the address selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	OFF	ON	OFF	ON	OFF	OFF

- (d) Check that the INTERRUPT SELECTOR is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF

- (e) Check that the power rails to the External Sync Control Board are as follows:

SKT 5	VOLTAGE	
A. 4	0V	GROUP 1
A. 3	0V	
A. 2	+5V	
A. 1	+5V	

LINK 1, LINK 4, LINK 6, OUT
LINK 2, LINK 3, LINK 5, IN

If these are correct, renew the External Sync Control Board.

5.6. Communications Interface, SKT 8 - G.P.I.B. Option SE 2451/00

- 5.6.1 If this option fails to operate correctly refer to Section 3 of the Communications and General Purpose Interface Bus Option SE2451/00 Manual for Link and Switch Settings.

Check that the power rails to the Communications Interface SKT 8 are as follows:

SKT 8	VOLTAGE	
A. 6	-12V	GROUP 1
A. 5	+12V	
A. 4	0V	
A. 3	0V	
A. 2	+ 5V	
A. 1	+ 5V	

If these are correct renew the Communications Interface Board.

5.7. Minimum System Configuration

The minimum system configuration for the SE 2450 is as follows:

DISPLAY CONTROL 1
 DISPLAY CONTROL 2
 PROCESSOR AND CURSOR CONTROL
 MEMORY
 KEYBOARD
 PSU
 MONITOR MODULE
 CHASSIS

In this configuration the display should appear. The data entry pages can be set up but when the START key is pressed the word DELAY is brightened and stays on due to the absence of correlator A interrupts. The only way to recover control in this situation is to press the RESET switch on the control panel.

MEMORY AND PROCESSOR CURSOR CONTROL BOARD CHECKS.

- (a) The contents of the PROMs can be checked by pressing SHIFT 9 on the keyboard. Depending on the software version installed, they should read:

		SE 2461/03 Software		SE 2462/01 Software	
0	0000	4EC4	(IC18C)	FE74	(IC18C)
1	0800	5174	(IC17C)	AA48	(IC17C)
2	1000	71D7	(IC16C)	8656	(IC16C)
3	1800	DE57	(IC15C)	01C6	(IC15C)
4	2000	23B0	(IC13C)	EFF8	(IC13C)
5	2800	4A79	(IC11C)	87A9	(IC11C)
6	3000	70E5	(IC10C)	F000	-
7	3800	7CB9	(IC 8C)	F000	-
8	4000	3370	(IC 7C)	-	-
9	4800	3122	(IC 5C)	-	-
10	5000	F800	-	-	-
11	5800	F800	-	-	-
12	6000	F800	-	-	-
13	6800	F800	-	-	-
14	7000	F800	-	-	-
15	7800	F800	-	-	-

(b) Check that the power rails to the Memory Board are as follows:

SKT 10	VOLTAGE	
A 6	- 12V	GROUP 1
A 5	+ 12V	
A 4	0V	
A 3	0V	
A 2	+ 5V	
A 1	+ 5V	

(c) Check that the power rails on the Processor and Cursor Control Board are as follows:

SKT 9	VOLTAGE	
A 6	- 12V	GROUP 1
A 5	+ 12V	
A 4	0V	
A 3	0V	
A 2	+ 5V	
A 1	+ 5V	

(d) Check that the address selector is set as follows:

S8	S7	S6	S5	S4	S3	S2	S1
OFF	OFF	ON	ON	ON	ON	OFF	OFF

If any Data Page is corrupted, the fault probably exists on either the Memory or the Processor Board.

The Processor and Memory Boards should also be checked out, if any of the following units have been renewed:

Correlator A/D Board
Correlator Control Board
Generator A/D Board
Generator Control Board
External Sync Control Board
Communications GPIB Interface Board
Keyboard

5.8. Power Supply

If the power rails are suspect, refer in the first instance, to page 4.18, fig. 4.11 to identify the power supply groups and their relevant fuses.

SECTION 8

CIRCUIT & COMPONENT LAYOUT DIAGRAMS

Dwg. No.	LIST OF COMPONENTS	Fig No.
<i>Plug-In P.C. Boards</i>		
	Processor & Cursor Control Board	
E 82025	- Circuit Diagram (sheet 1)	8.1
E 82025	- Circuit Diagram (sheet 2)	8.2
D 82026	- Assembly Diagram	8.3
	Memory Boards	
E 82020	- Circuit Diagram	8.4
D 82021	- Assembly Diagram	8.4A
E 90917	- Circuit Diagram	8.5
D 82021/02	- Assembly Diagram	8.5A
	Generator Control Board	
E 82000	- Circuit Diagram	8.5
D 82001	- Assembly Diagram	8.7
	Generator D/A Boards	
E 82035	- Circuit Diagram	8.8
E 88662	- Circuit Diagram	8.8A
D 82036/01	- Assembly Diagram	8.9A
D 82036	- Assembly Diagram	8.9
	Correlator Control Board	
E 82005	- Circuit Diagram	8.10,8.10A
D 82006	- Assembly Diagram	8.11,8.11A
	Correlator A/D Board	
E 82040	- Circuit Diagram	8.12
D 82041	- Assembly Diagram	8.13
	Display Control 1 Board	
E 82050	- Circuit Diagram	8.14
D 82051	- Assembly Diagram	8.15
	Display Control 2 Board	
E 82055	- Circuit Diagram	8.16
D 82056	- Assembly Diagram	8.17
	Alphanumeric Control Board	
E 90220	- Circuit Diagram	8.17A
D 90221	- Assembly Diagram	8.17B
<i>Display Monitor</i>		
	Display Monitor TBK18V	
D 86901	- Circuit Diagram	8.18
C 86872	- Assembly Diagram	8.19
	CRT POT Board	
D 86901	- Circuit Diagram	8.18
B 86900	- Assembly Diagram	8.19

Keyboard

	Keyboard Logic Board	
E 82085	- Circuit Diagram	8.20
D 82086	- Assembly Diagram	8.21
	Keyswitch Board	
E 82085	- Circuit Diagram	8.20
D 82091	- Assembly Diagram	8.22
	Keyboard	
D 81222	- Assembly Diagram	8.23

Power Supply Unit

	Power Supply Board No.1	
E 82070	- Circuit Diagram	8.24
D 82071	- Assembly Diagram	8.26
	Power Supply Board No.2	
E 82070	- Circuit Diagram	8.24
D 82076	- Assembly Diagram	8.27
	Power Supply Motherboard	
E 82070	- Circuit Diagram	8.24
D 82081	- Assembly Diagram	8.28
	Power Supply Unit	
E 81221	- Assembly Diagram	8.25

FRA Motherboard,Control & Input Panels

E 82061	- Assembly Diagram	8.29
-	- External Connections (with Control & I/P Panels)	8.30
E 82060	- Internal Bus Connections (socket sides A)	8.31
E 82060	- Internal Bus Connections (socket sides B)	8.32

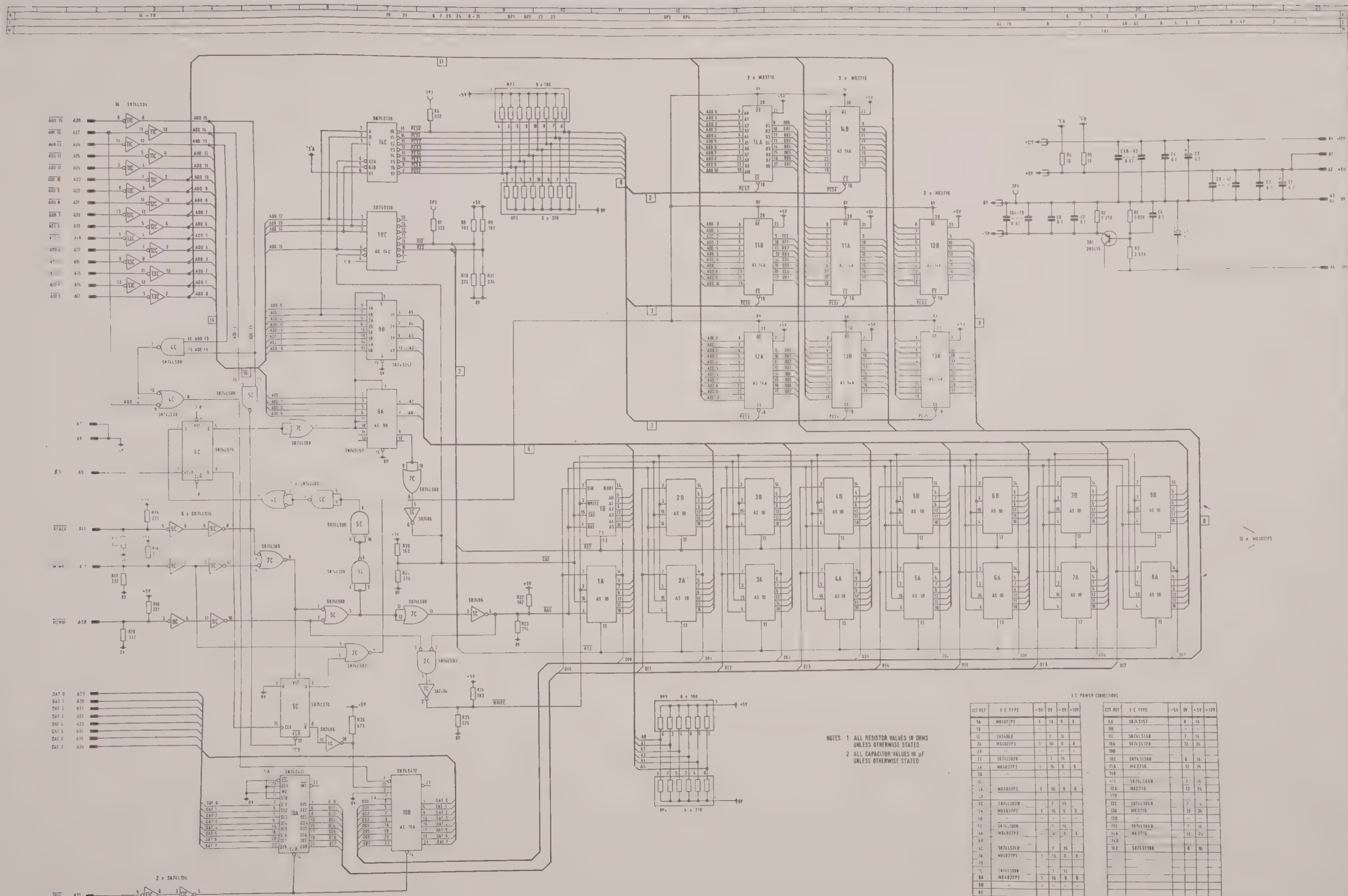
-	<i>FRA Cableform Interconnections</i>	8.33
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FREQUENCY RESPONSE ANALYSER SE2450
PROCESSOR & CURSOR CONTROL BOARD - sht 2

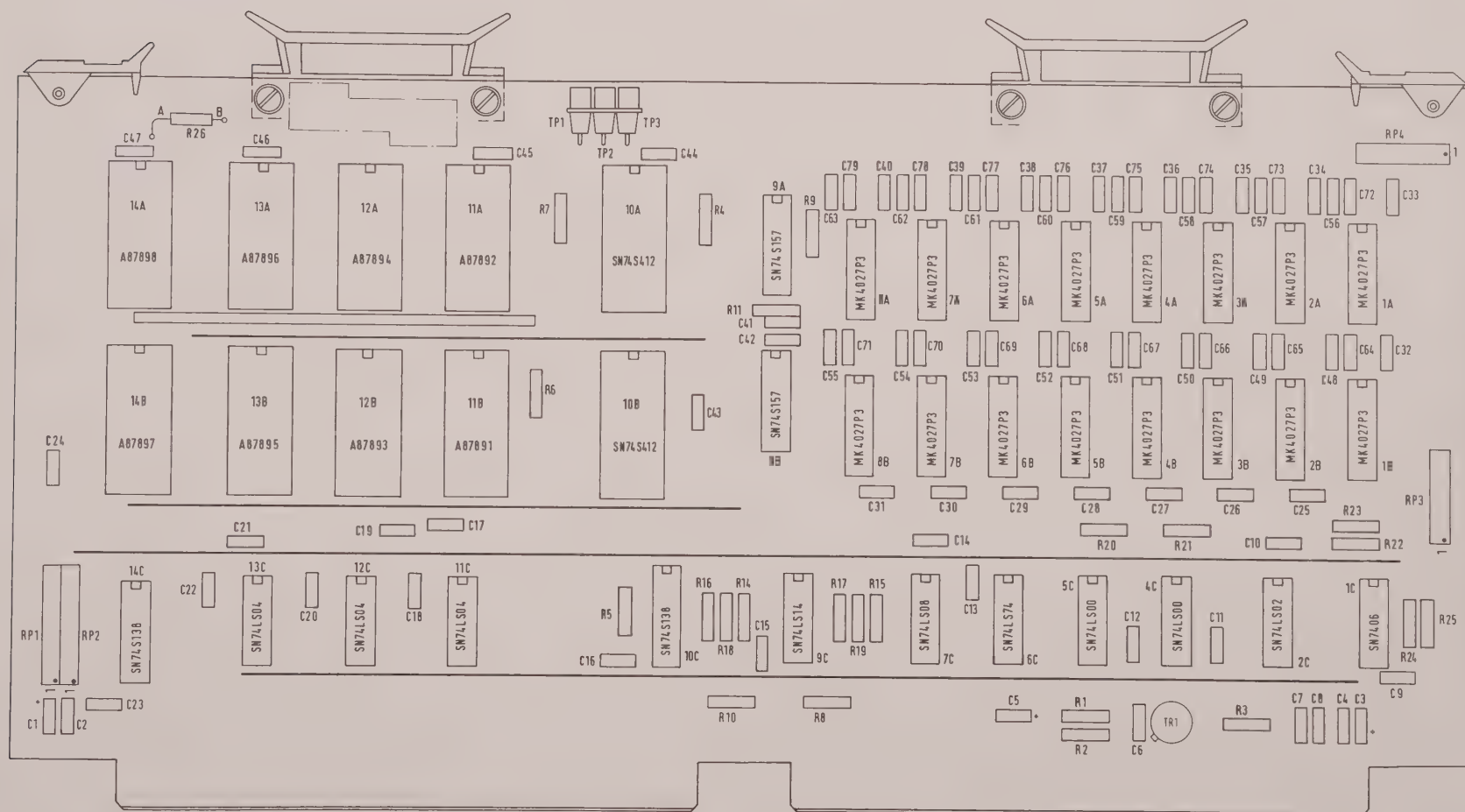
FIG. 8.2
E82025
ISSUE 5



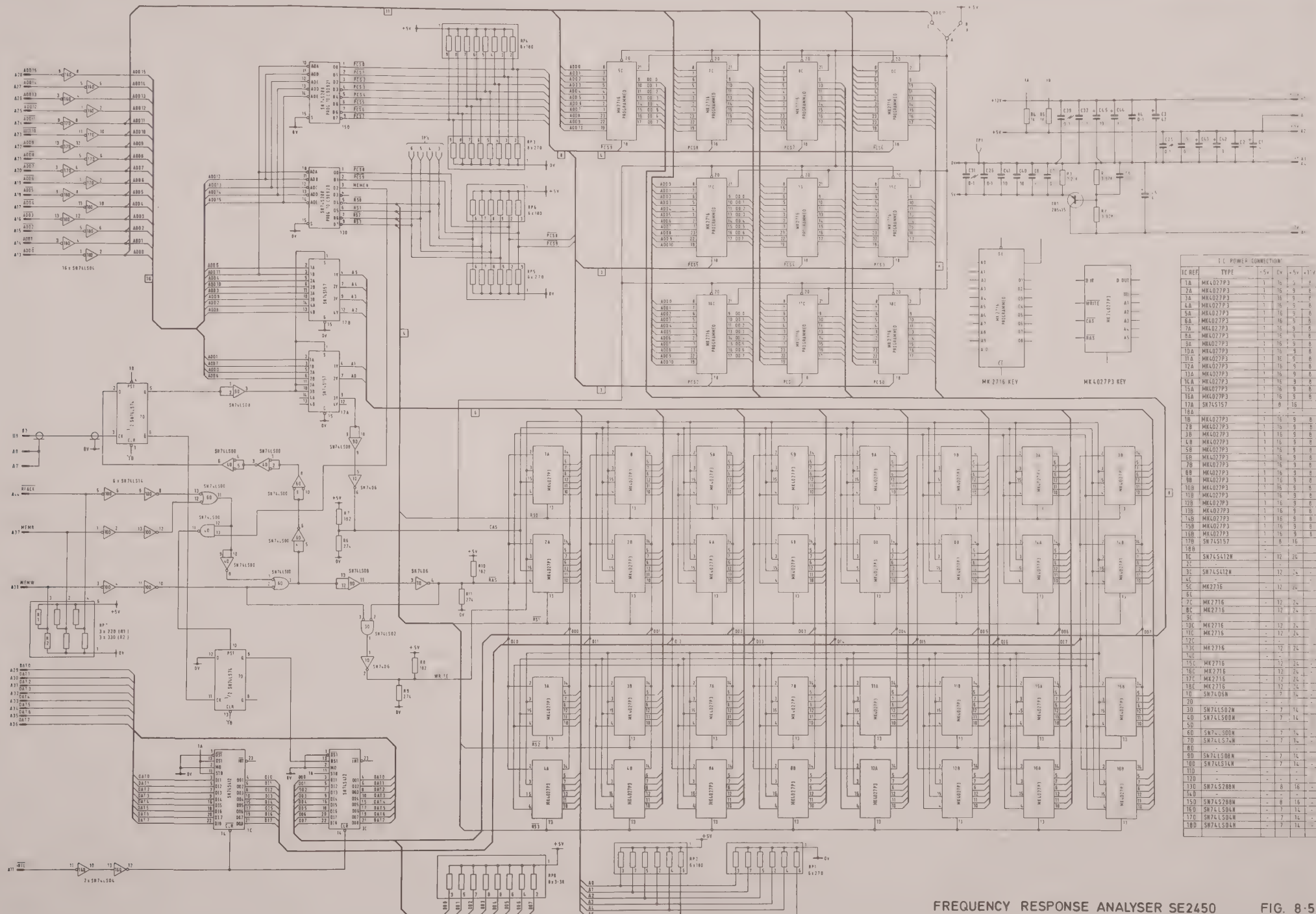


FREQUENCY RESPONSE ANALYSER SE2450
MEMORY BOARD

FIG. 8.4
EB2020
ISSUE 3



FREQUENCY RESPONSE ANALYSER SE2450
MEMORY BOARD



FREQUENCY RESPONSE ANALYSER SE2450
MEMORY 2 BOARD

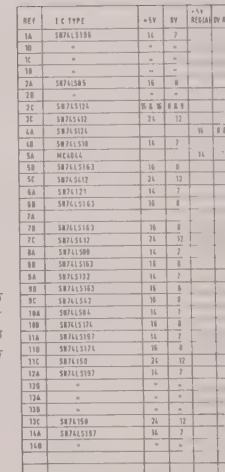
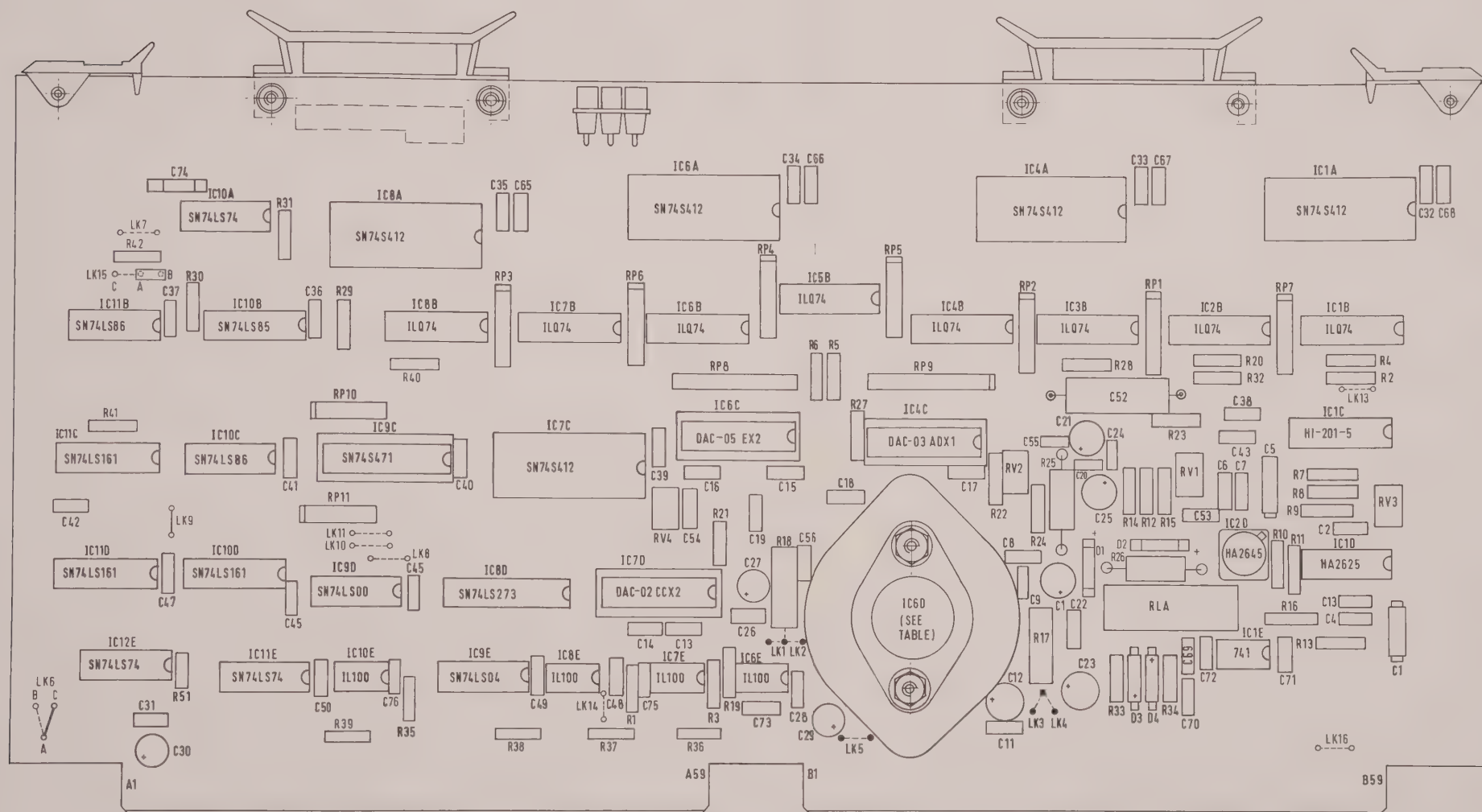


FIG. 8.6
E82000
ISSUE 7



FIG. 8.7
D82001
ISSUE 9

A	AP1	1	2	3	AP2	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219	12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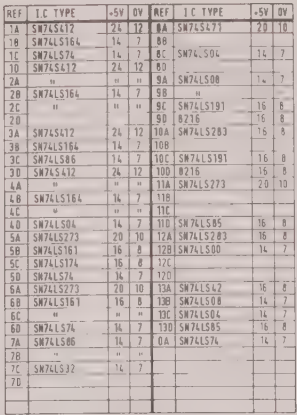


IC6D	
TYPE	LINK POSITIONS
BB3571	LINK 1 AND LINK 3
BB3573	LINK 2 AND LINK 4

FREQUENCY RESPONSE ANALYSER SE2450
GENERATOR D/A. BOARD

FIG.8.9A
D82036/01
ISSUE 4





FREQUENCY RESPONSE ANALYSER SE2450
CORRELATOR CONTROL BOARD

FIG. 8.10
E82005
ISSUE 6

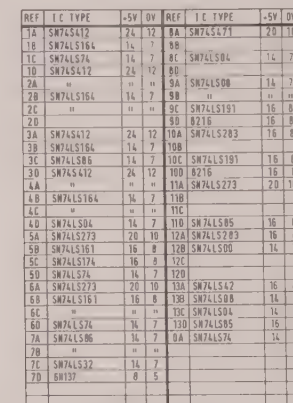
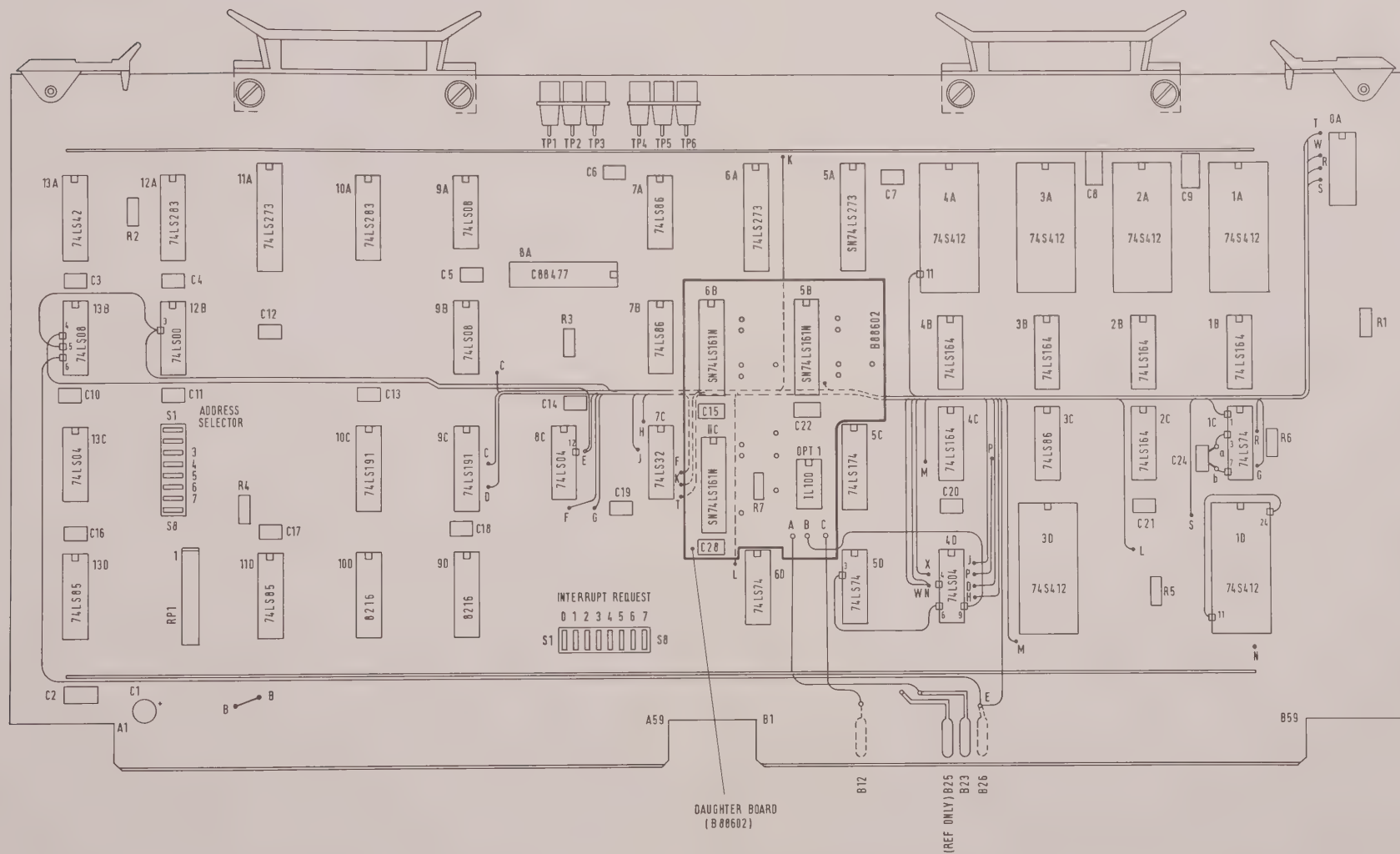
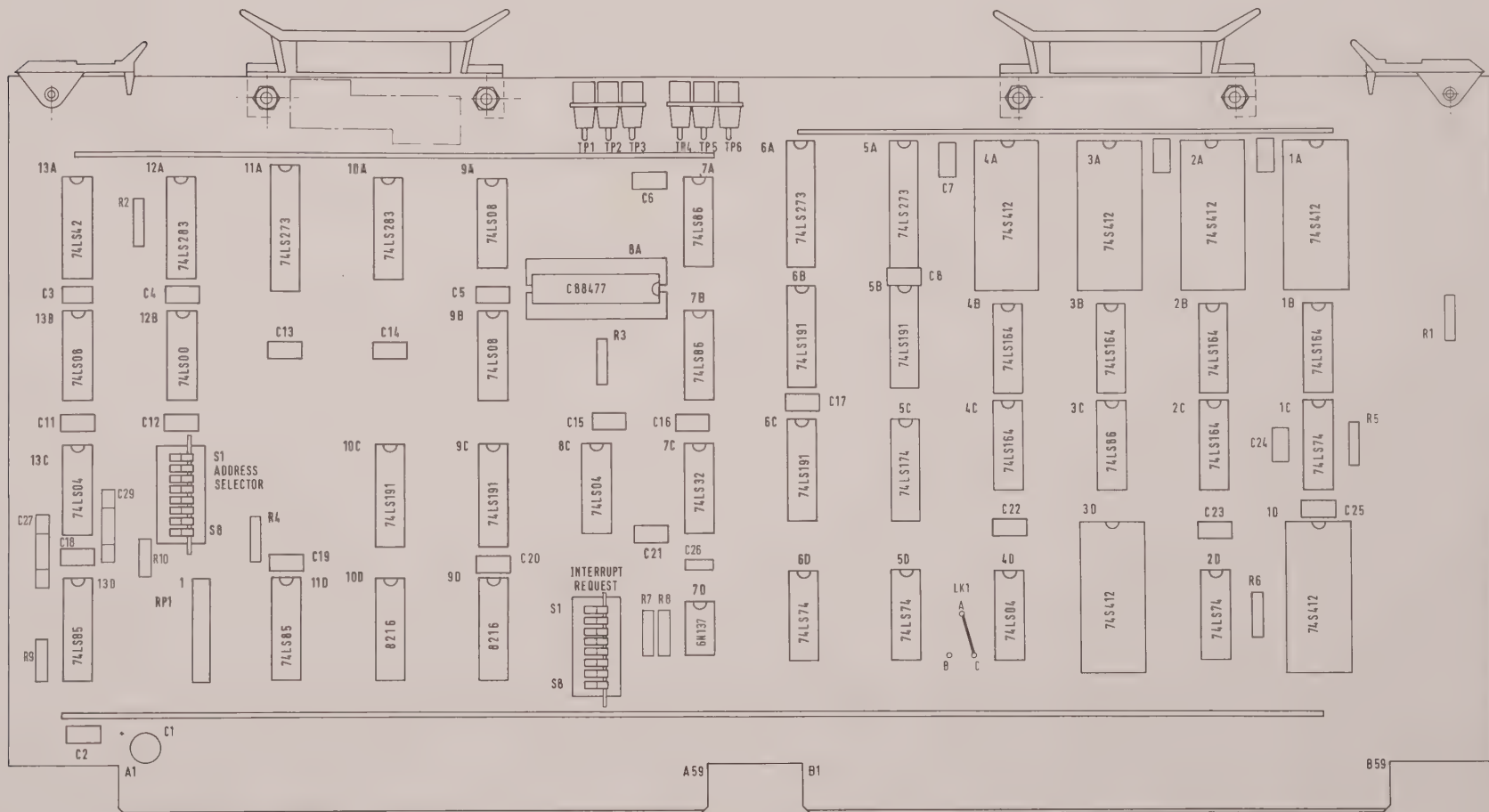


FIG.8.10A
E82005
ISSUE 8



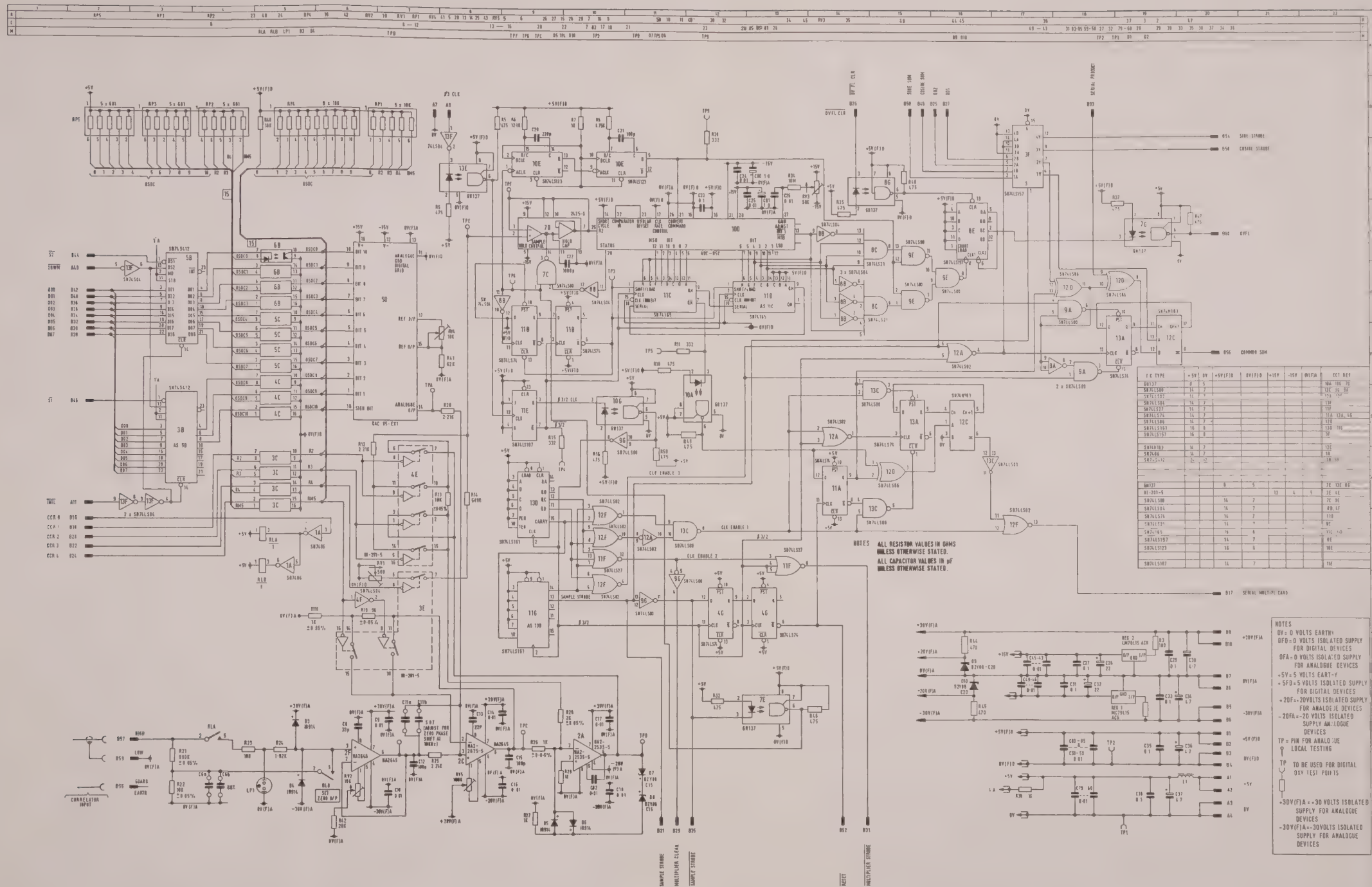
FREQUENCY RESPONSE ANALYSER SE2450
CORRELATOR CONTROL BOARD

FIG. 8.11
D82006
ISSUE 3

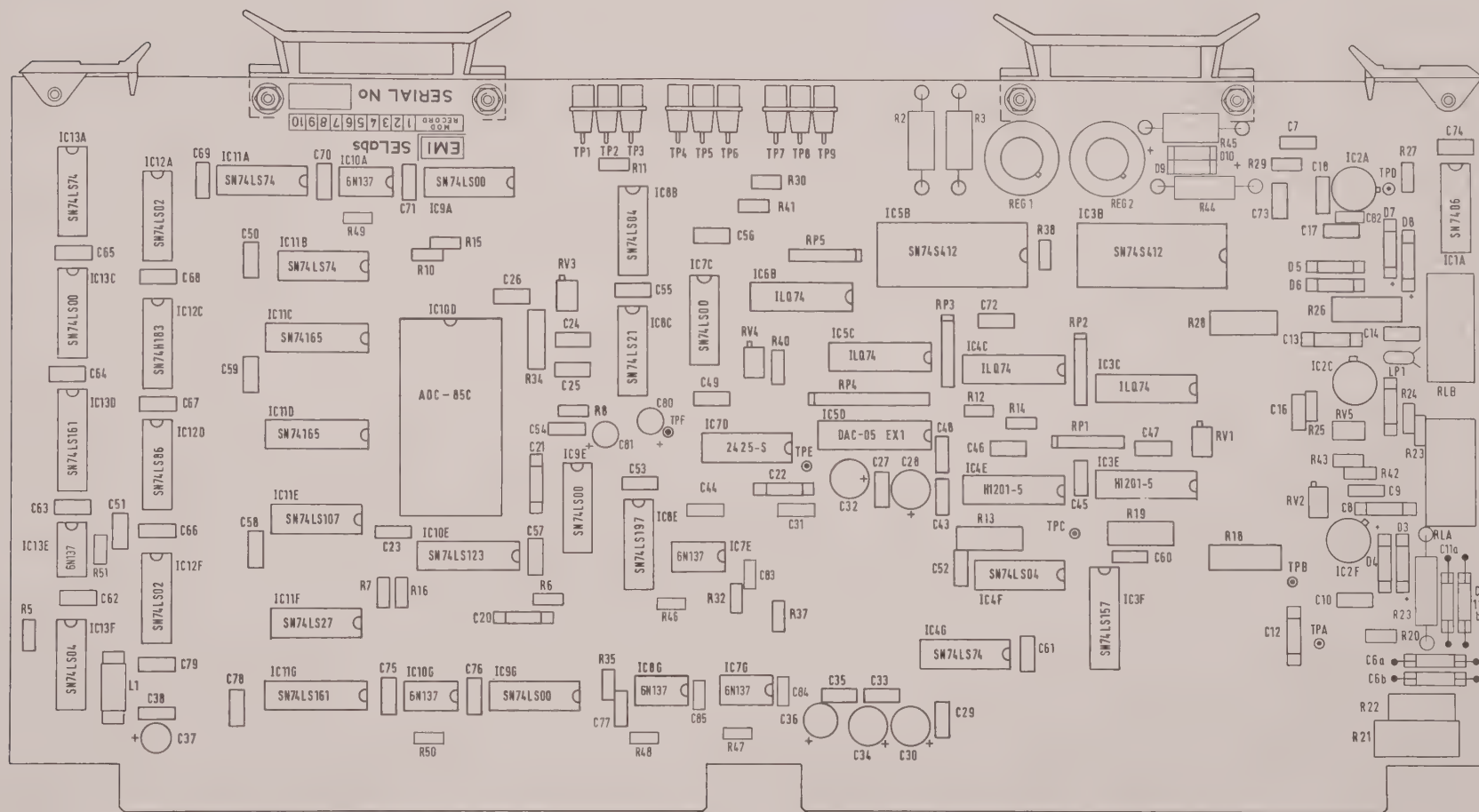


FREQUENCY RESPONSE ANALYSER SE 2450 FIG 8.11A

CORRELATOR CONTROL BOARD D82006
ISSUE 10

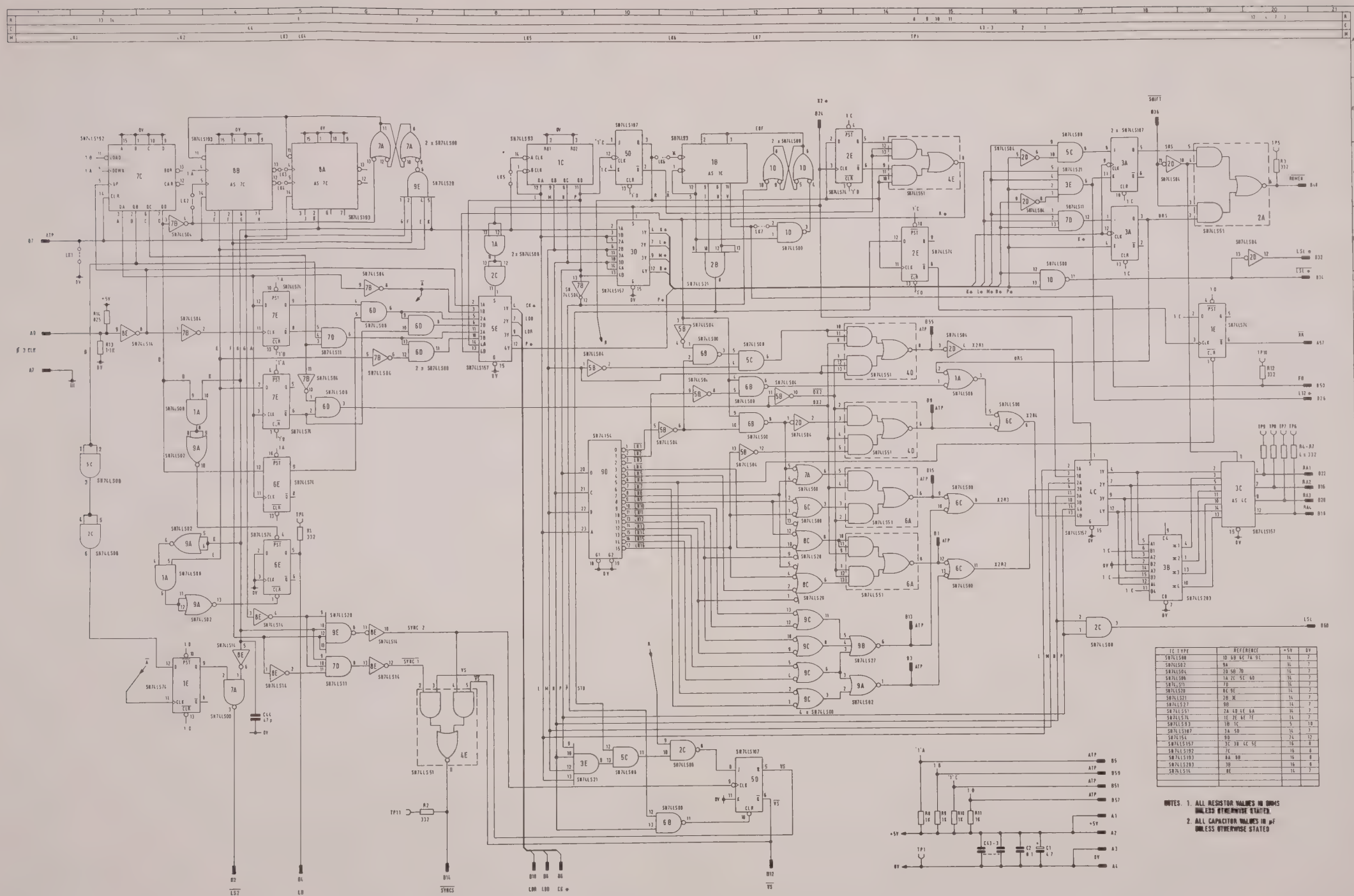


FREQUENCY RESPONSE ANALYSER SE2450
 CORRELATOR A/D BOARD



FREQUENCY RESPONSE ANALYSER SE2450
CORRELATOR A/D BOARD

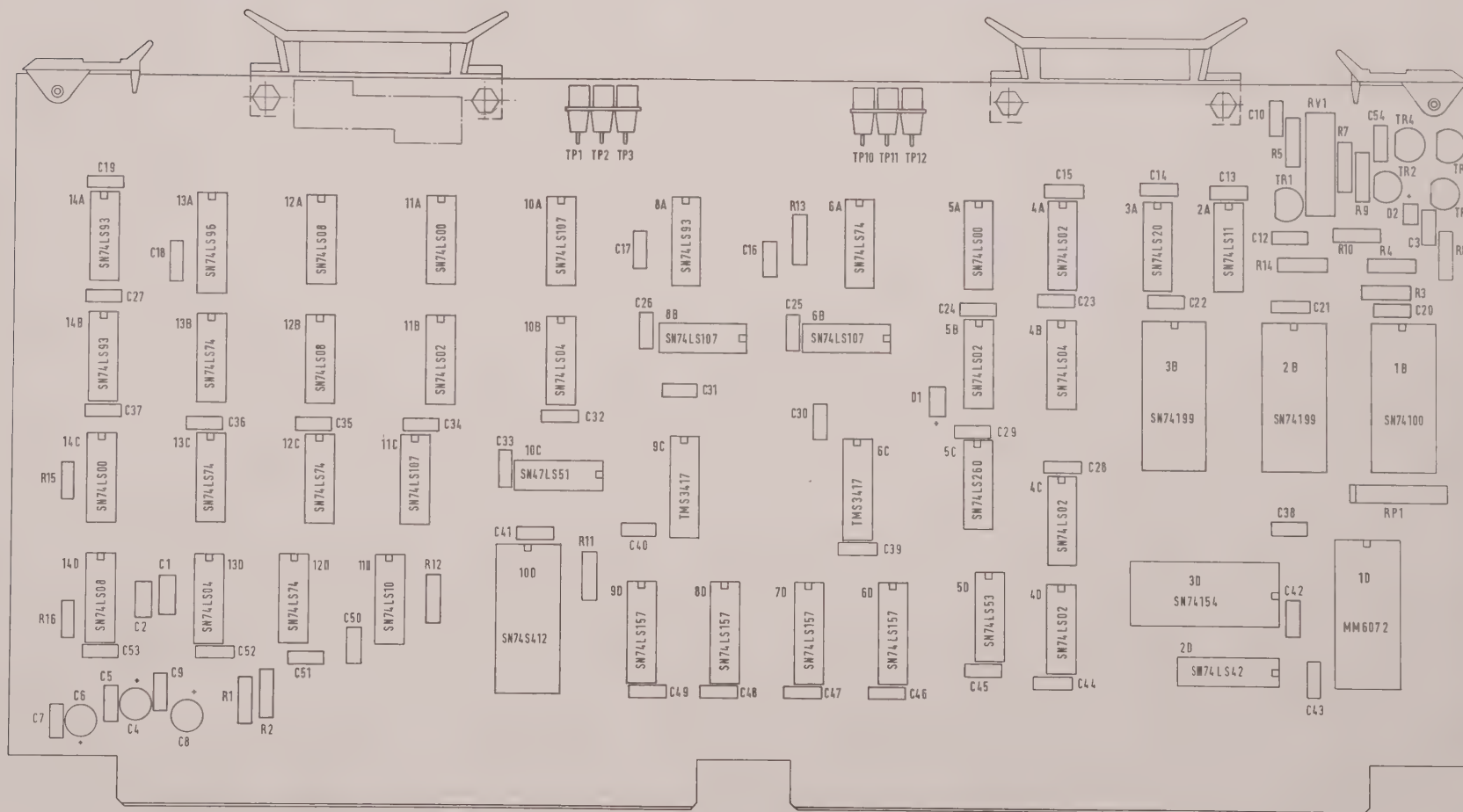
FIG. 8.13
D82041
ISSUE 8



FREQUENCY RESPONSE ANALYSER SE2450
DISPLAY CONTROL 1 BOARD

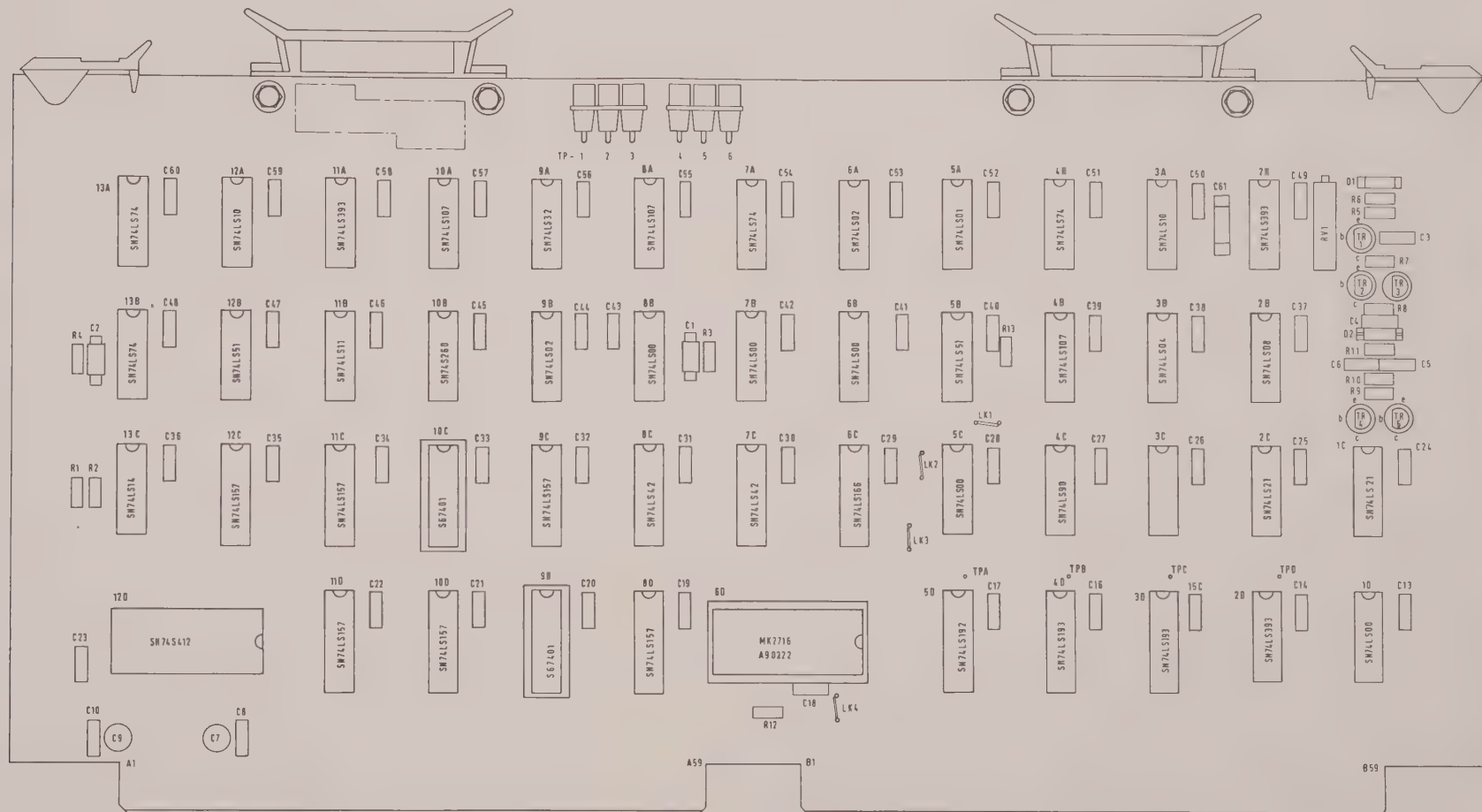


FIG. 8.15
D82051
ISSUE 6

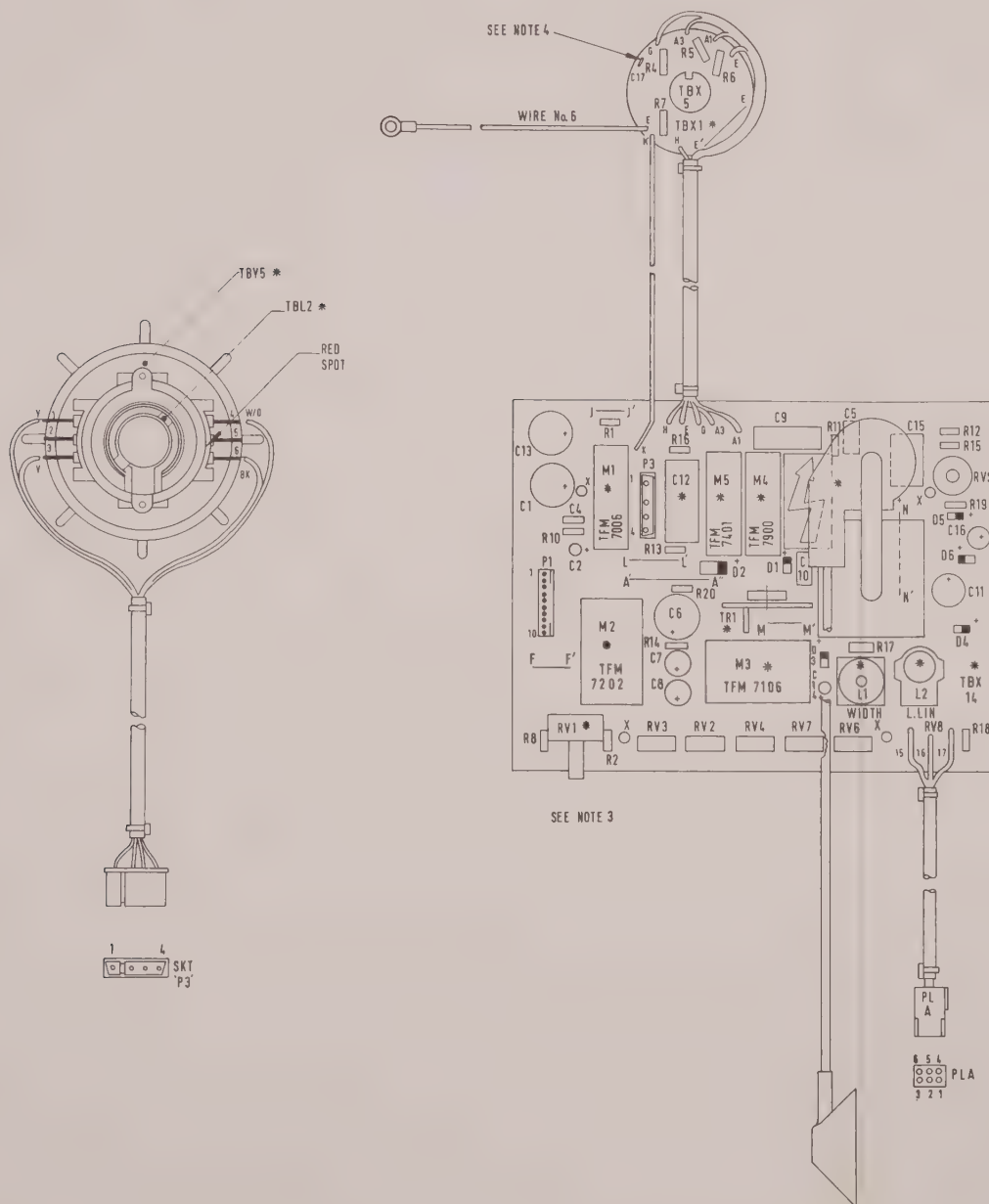


FREQUENCY RESPONSE ANALYSER SE2450
DISPLAY CONTROL 2 BOARD

FIG. 8.17
D82056
ISSUE 3



ALPHANUMERIC CONTROL BOARD
 COMPONENT LAYOUT
 FIG. 8.17B
 D90221
 ISSUE 2

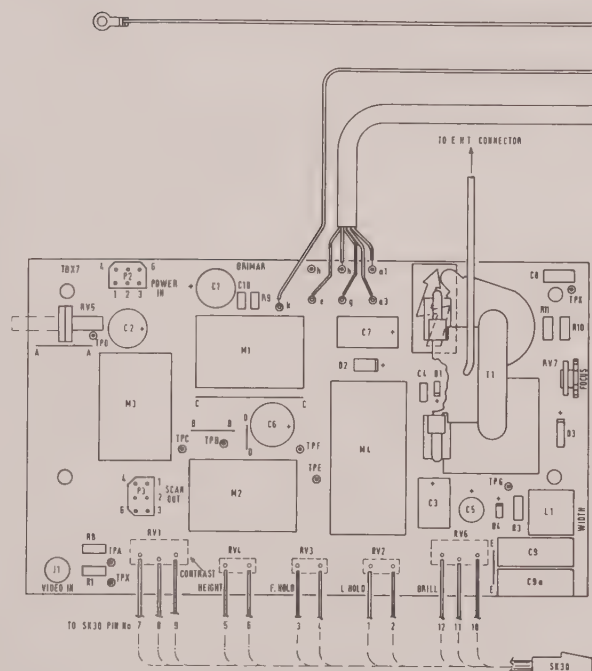


WIRING SCHEDULE										
WIRE No	WIRE DETAILS			FROM			TO			REMARKS
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2	BL	16/0-2	82		TBX1	E	TBX14		E	
3	GN	16/0-2	83		TBX1	A1	TBX14		A1	
4	YL	16/0-2	84		TBX1	A3	TBX14		A3	
5	V	16/0-2	85		TBX1	G	TBX14		G	
6	BL	16/0-2	82		TBX1	E	EARTH TAG		—	EARTH
7	WH/OR	16/0-2	86		TBX1	K	TBX14		K	
8	YL	16/0-2	84		TBY5	1	SKT.P3		4	
9	V	16/0-2	85		TBY5	3	SKT.P3		3	
10	WH/OR	16/0-2	86		TBY5	4	SKT.P3		1	
11	BK	16/0-2	87		TBY5	6	SKT.P3		2	
12										
13										
14										
15	BK/OR	16/0-2	90		TBX14	RV8	PLA		6	
16	BL/BN	16/0-2	91		TBX14	RV8	PLA		5	
17	BL/OR	16/0-2	92		TBX14	RV8	PLA		4	

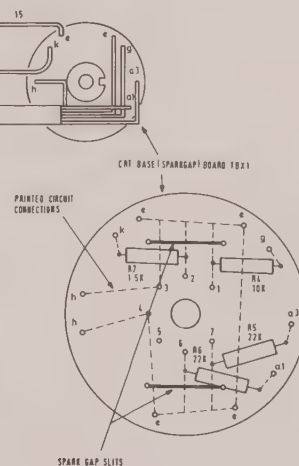
- NOTES
- ITEMS MARKED THUS: * ARE PART OF MONITOR MODULE KIT ITEM 5
 - RV1, RV8, R3, R9, C3 SKT 2, TPs LK B-B' & LK A-A' ARE NOT FITTED
 - SPINDLE LENGTH OF RV1 TO BE CUT DOWN TO 12MM MIN/15MM MAX
 - C17 IS FITTED BETWEEN 'E' & 'G' HOLES ON TBX1*

FREQUENCY RESPONSE ANALYSER
DISPLAY MONITOR BRIMAR 29A
FIG 8.19A
D86872/01
ISSUE 2

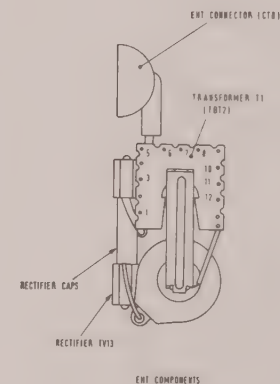
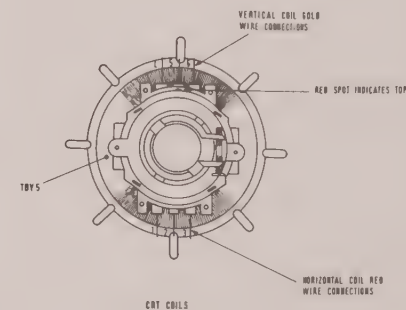
COLOUR CODE FOR SK30	
CLOUR	P.W.No
RED/BA	6
RED/BLK	5
RED/BLU	3
GREY	4
BLACK	7
RED	1
WH/OR	7
WH/BLU	8
RED/BRN	9
BL/OR	10
BL/BRN	11
BR/OR	12
YEL/GRN	EARTH



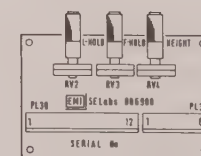
VIDEO BOARD TBX1 C06072 ISSUE B



SPARK GAP SLITS



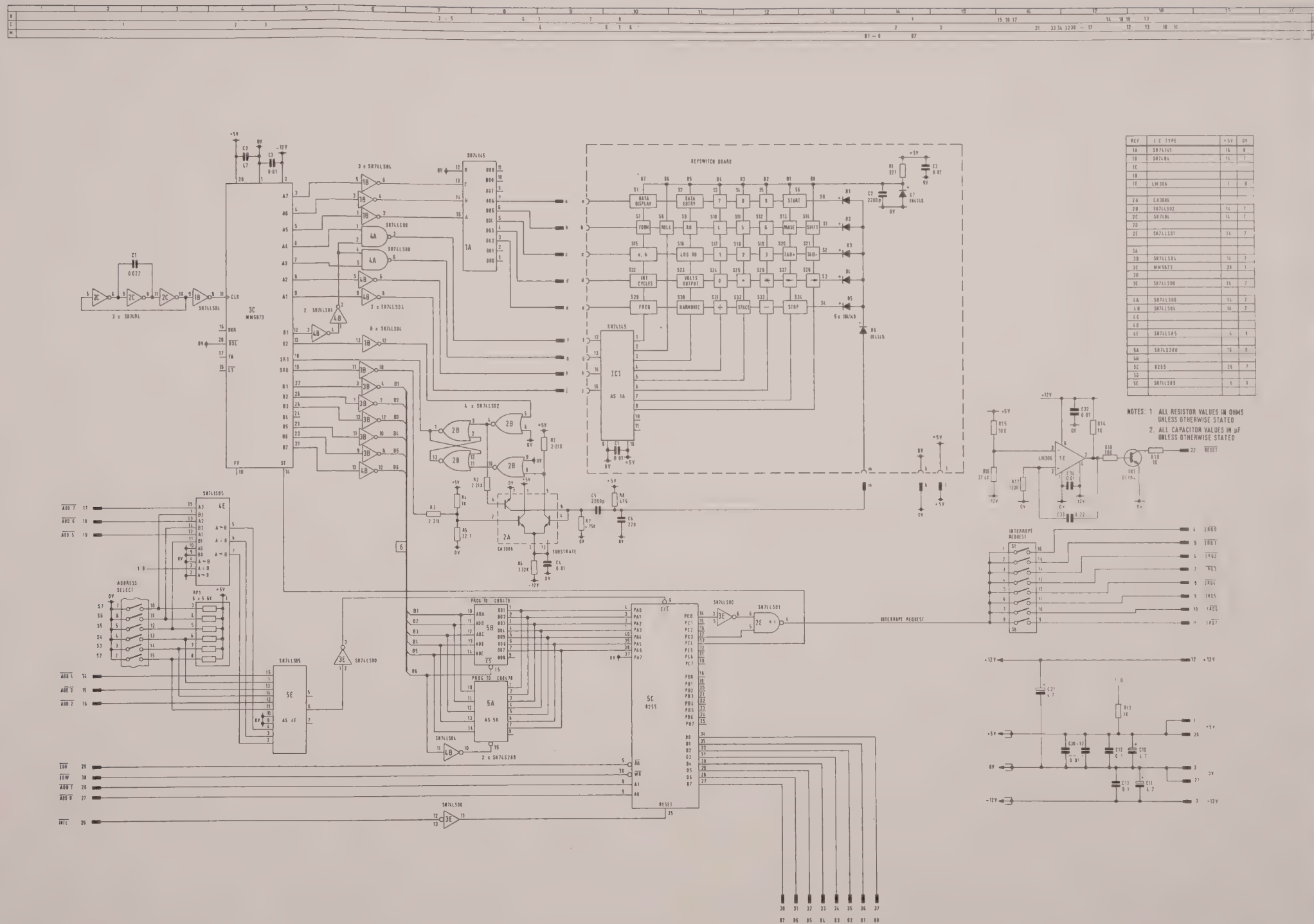
EHT COMPONENTS



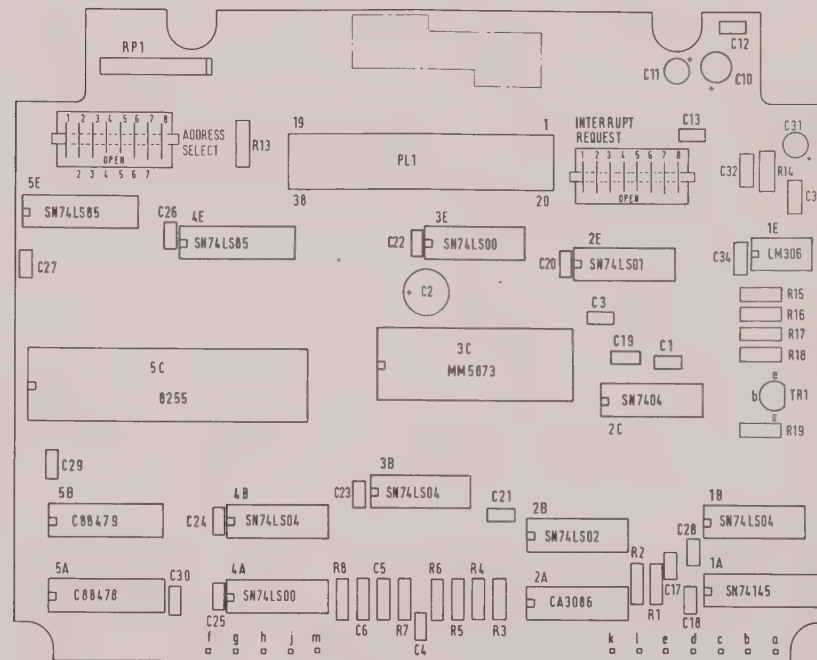
CRT POT BOARD D06500 ISSUE B

FREQUENCY RESPONSE ANALYSER SE2450
DISPLAY MONITOR TBK 18V

FIG.8.19

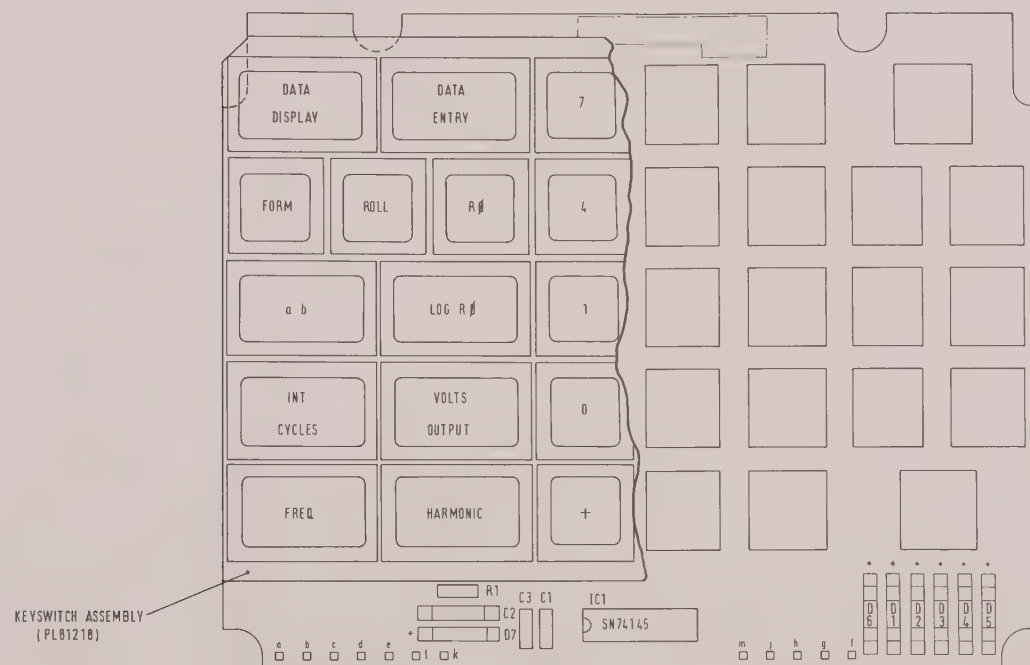


FREQUENCY RESPONSE ANALYSER SE2450
KEYBOARD



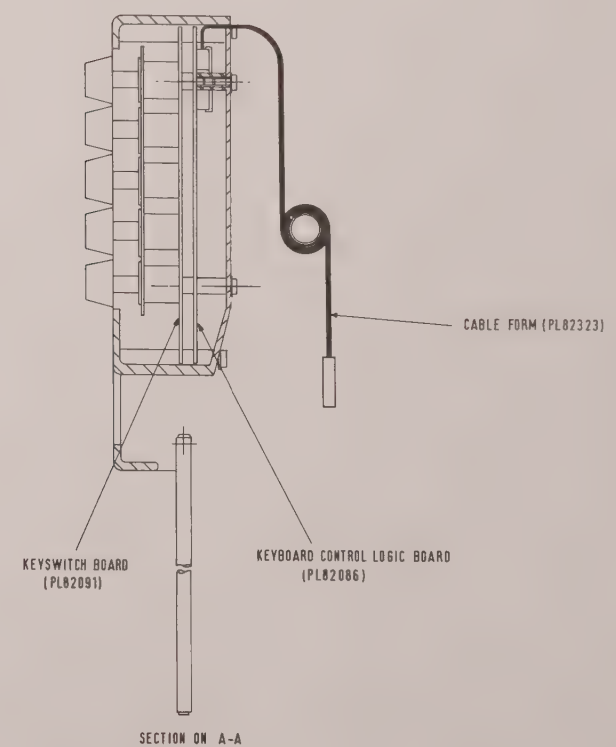
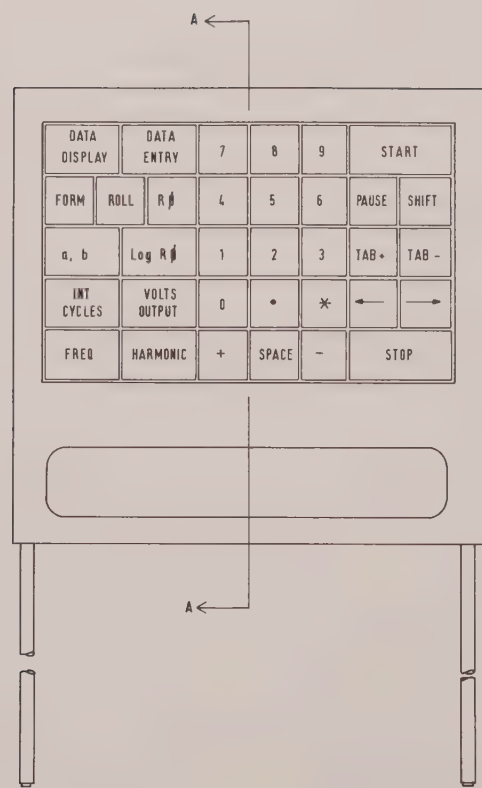
FREQUENCY RESPONSE ANALYSER SE2450
KEYBOARD CONTROL LOGIC BOARD

FIG. 8.21
D82086
ISSUE 8



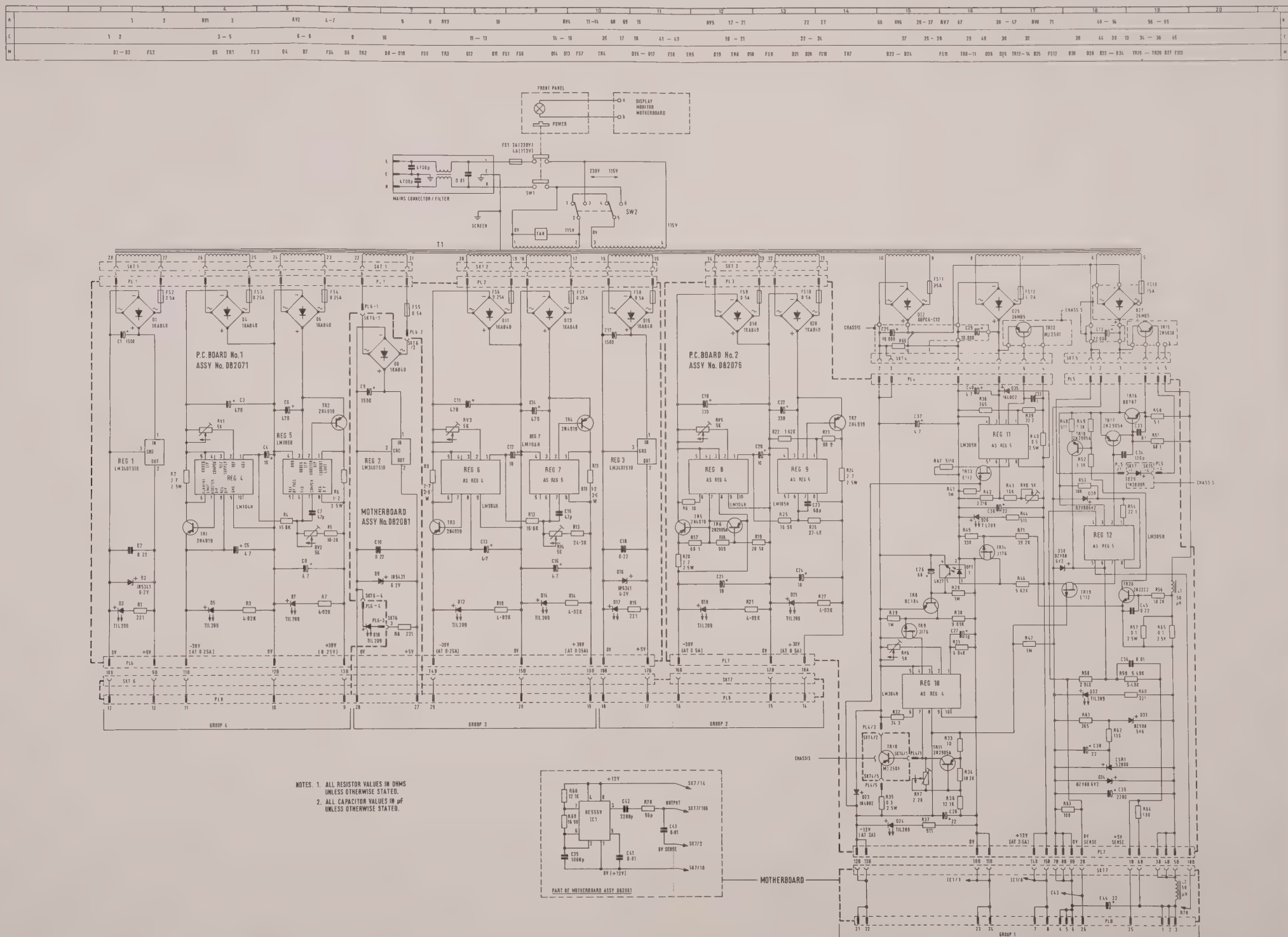
FREQUENCY RESPONSE ANALYSER SE2450
KEYSWITCH BOARD

NOTE
WHEN SOFTWARE IS UPDATED TO SE2450/D2 &
SE2450/D3 (SEE REAR PANEL), TAB+ & TAB-
KEY CAPS ARE TRANSPOSED

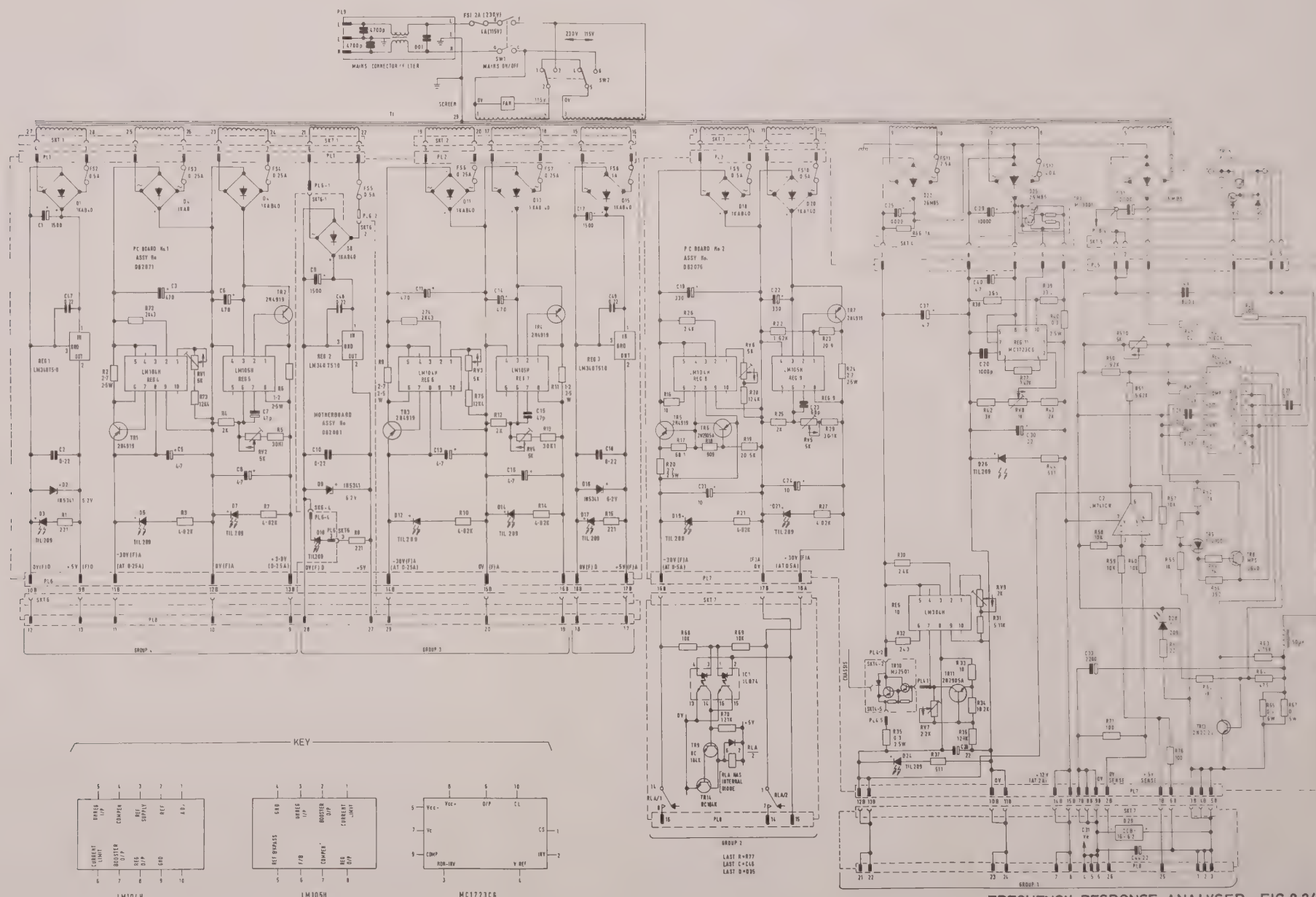


FREQUENCY RESPONSE ANALYSER SE2450
KEYBOARD

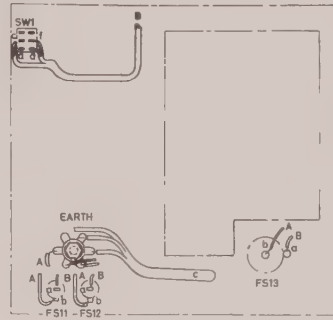
FIG. 8.23
D81222
ISSUE 4



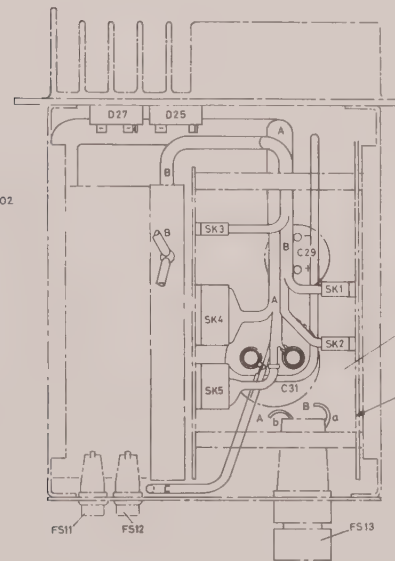
FREQUENCY RESPONSE ANALYSER SE2450
POWER SUPPLY



FREQUENCY RESPONSE ANALYSER FIG 8-24A
POWER SUPPLY 1 E92106

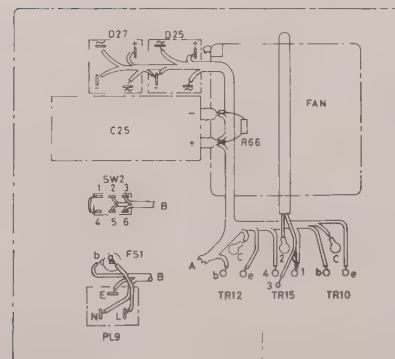
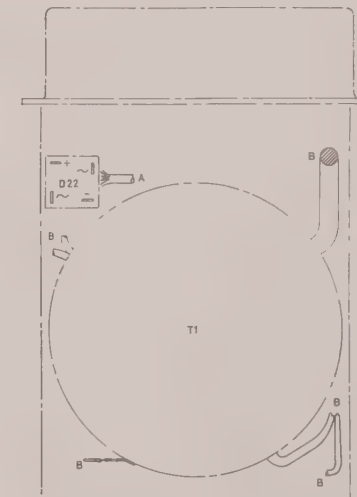


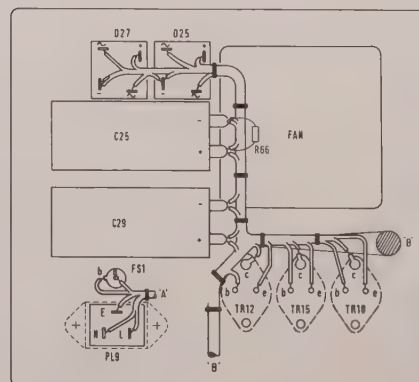
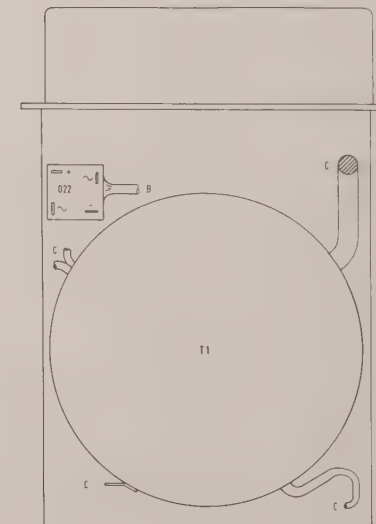
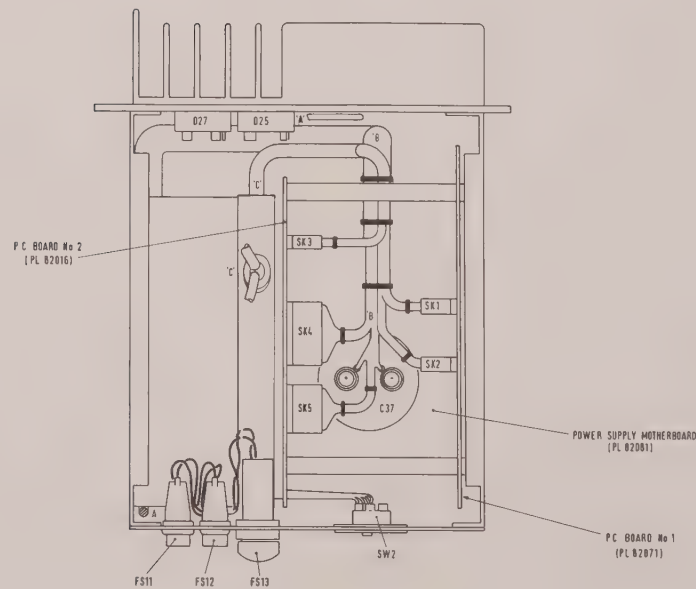
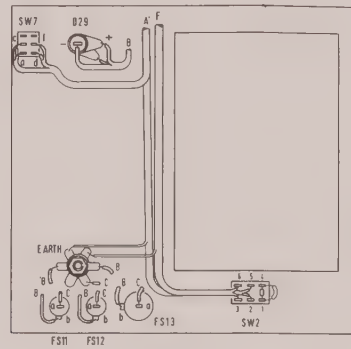
POWER SUPPLY BOARD NO2
(82076/01)



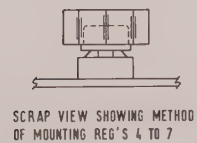
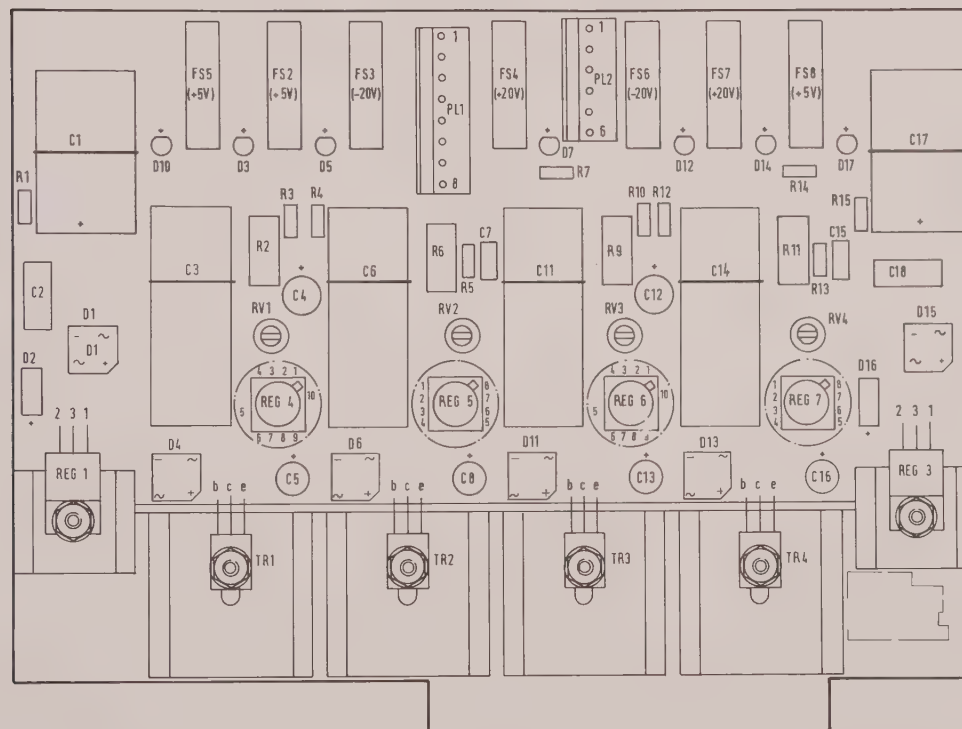
POWER MOTHERBOARD
(82081/01)

POWER BOARD NO1
(82071/01)

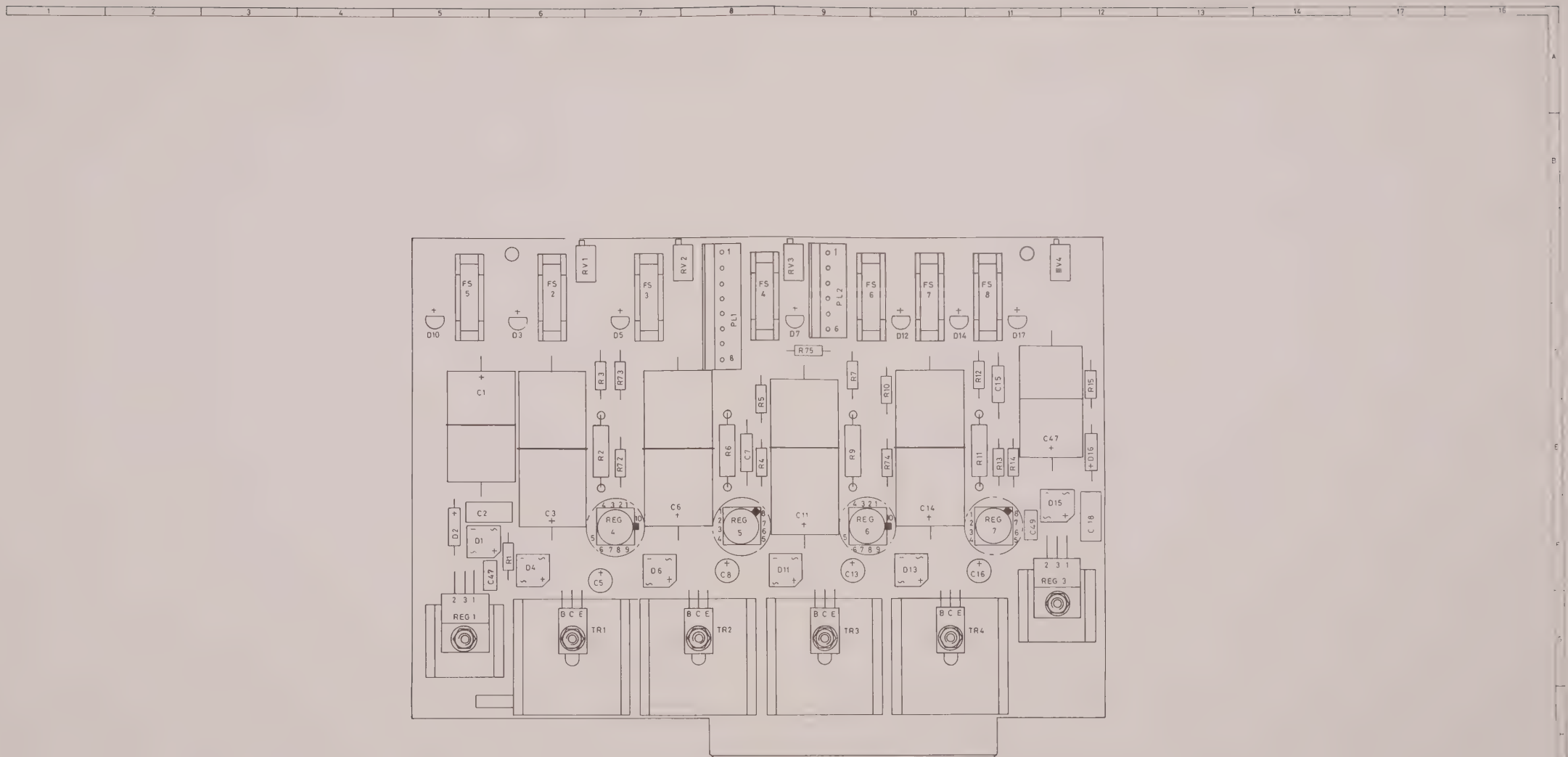




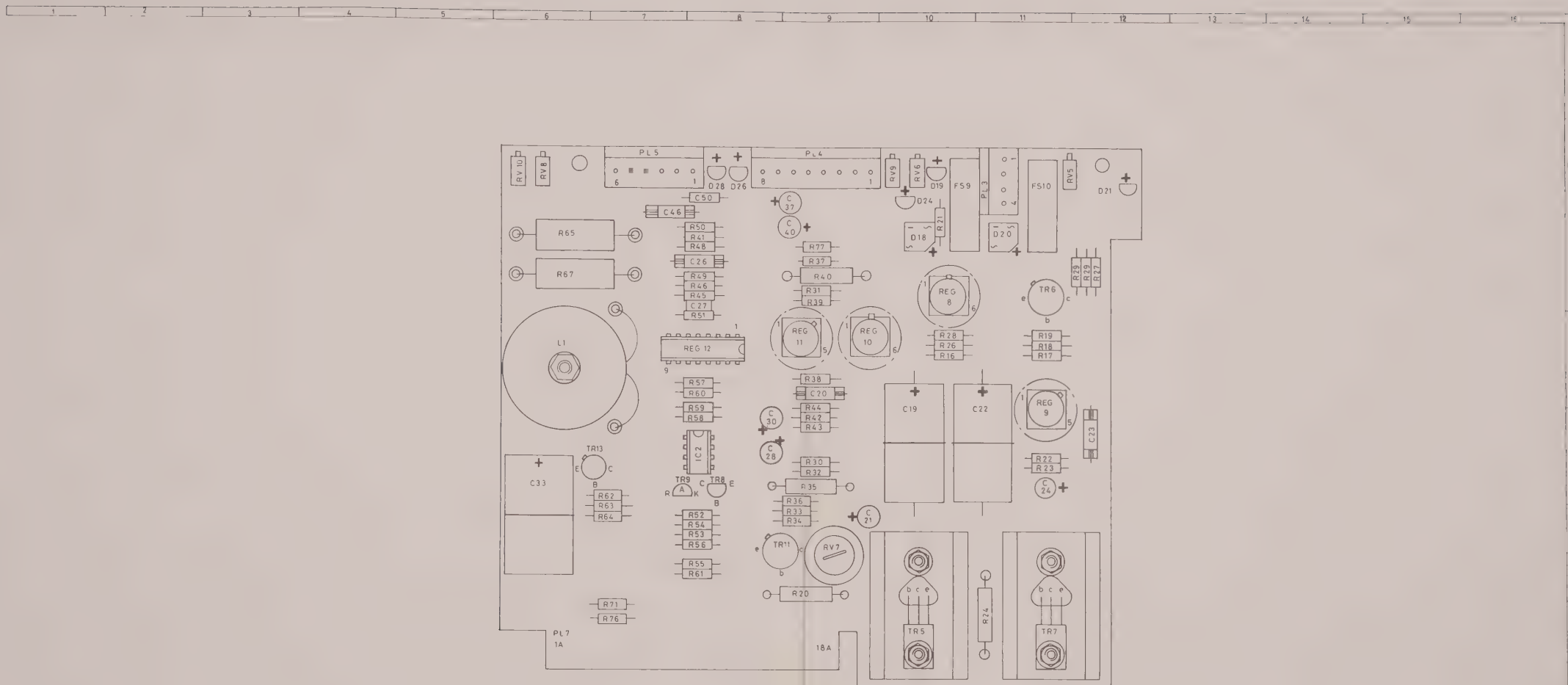
FREQUENCY RESPONSE ANALYSER SE2450
POWER SUPPLY (230V)



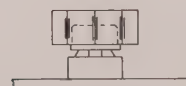
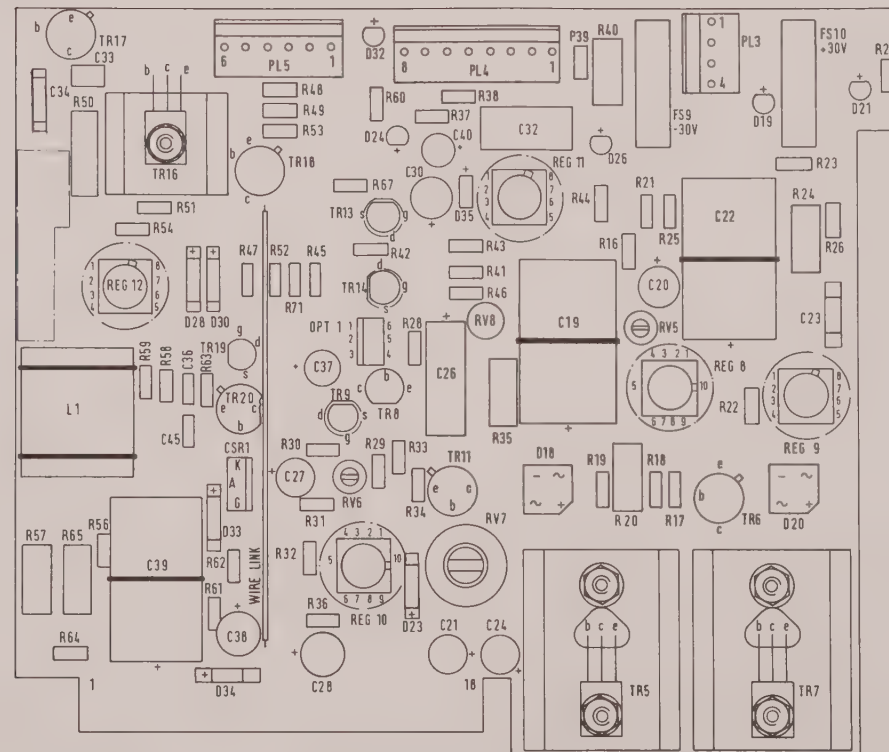
FREQUENCY RESPONSE ANALYSER SE2450
POWER SUPPLY BOARD No. 1



FREQUENCY RESPONSE ANALYSER FIG8.26A
 POWER SUPPLY BOARD NO1 (TYPE 1) D82071/01
 ISSUE 2



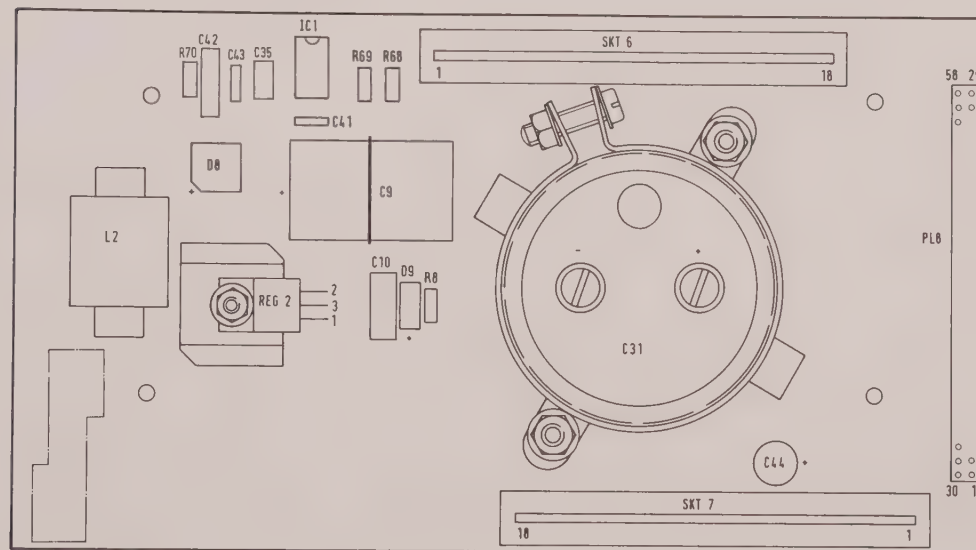
FREQUENCY RESPONSE ANALYSER FIG 8.27A
 POWER SUPPLY BOARD NO 2 (TYPE 1) D82076/01
 ISSUE 3



SCRAP VIEW SHOWING METHOD OF
MOUNTING REG'S 8 TO 12

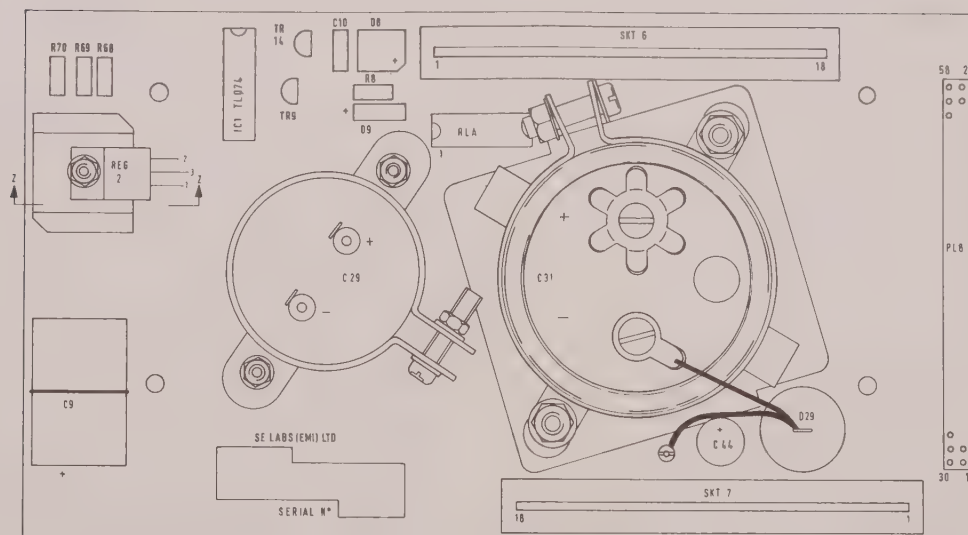
FREQUENCY RESPONSE ANALYSER SE2450
POWER SUPPLY BOARD No. 2

FIG. 8.27
D82076
ISSUE 5

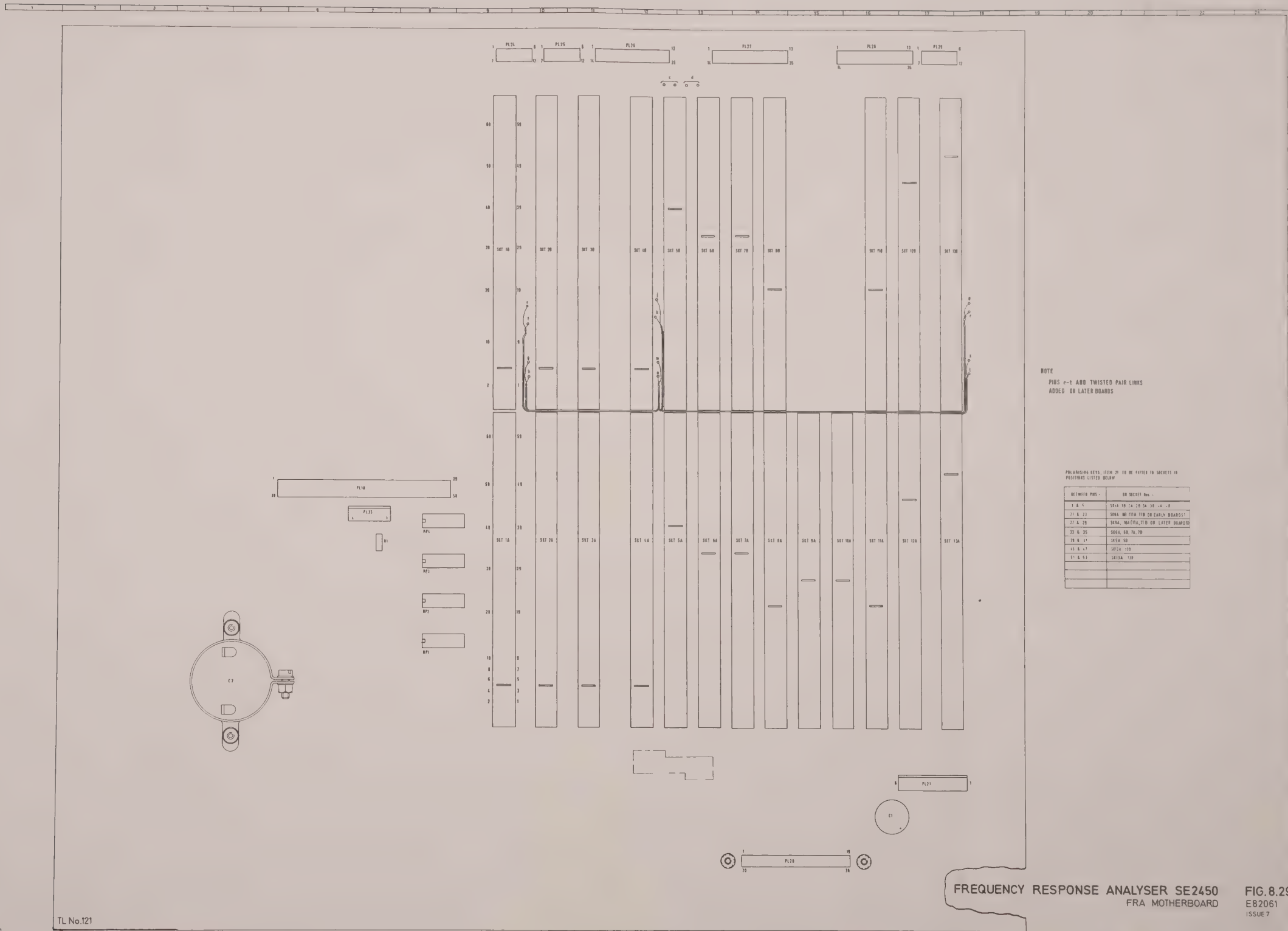


FREQUENCY RESPONSE ANALYSER SE2450
POWER SUPPLY MOTHERBOARD

FIG. 8.28
D82081
ISSUE 4



FREQUENCY RESPONSE ANALYSER FIG 8.28A
 POWER SUPPLY 1 MOTHERBOARD D82081/01
 ISSUE 3



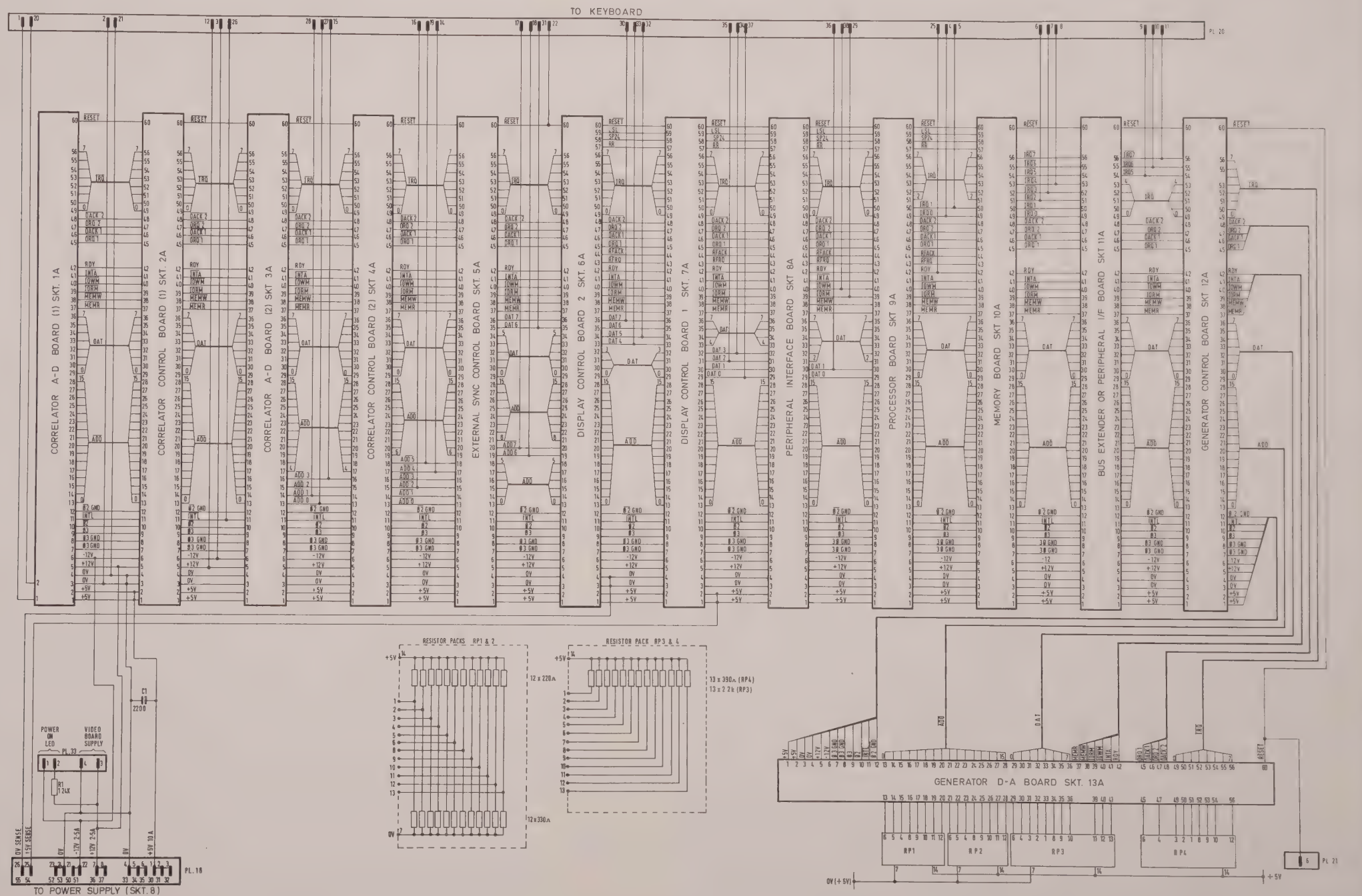
FRA MOTHERBOARD

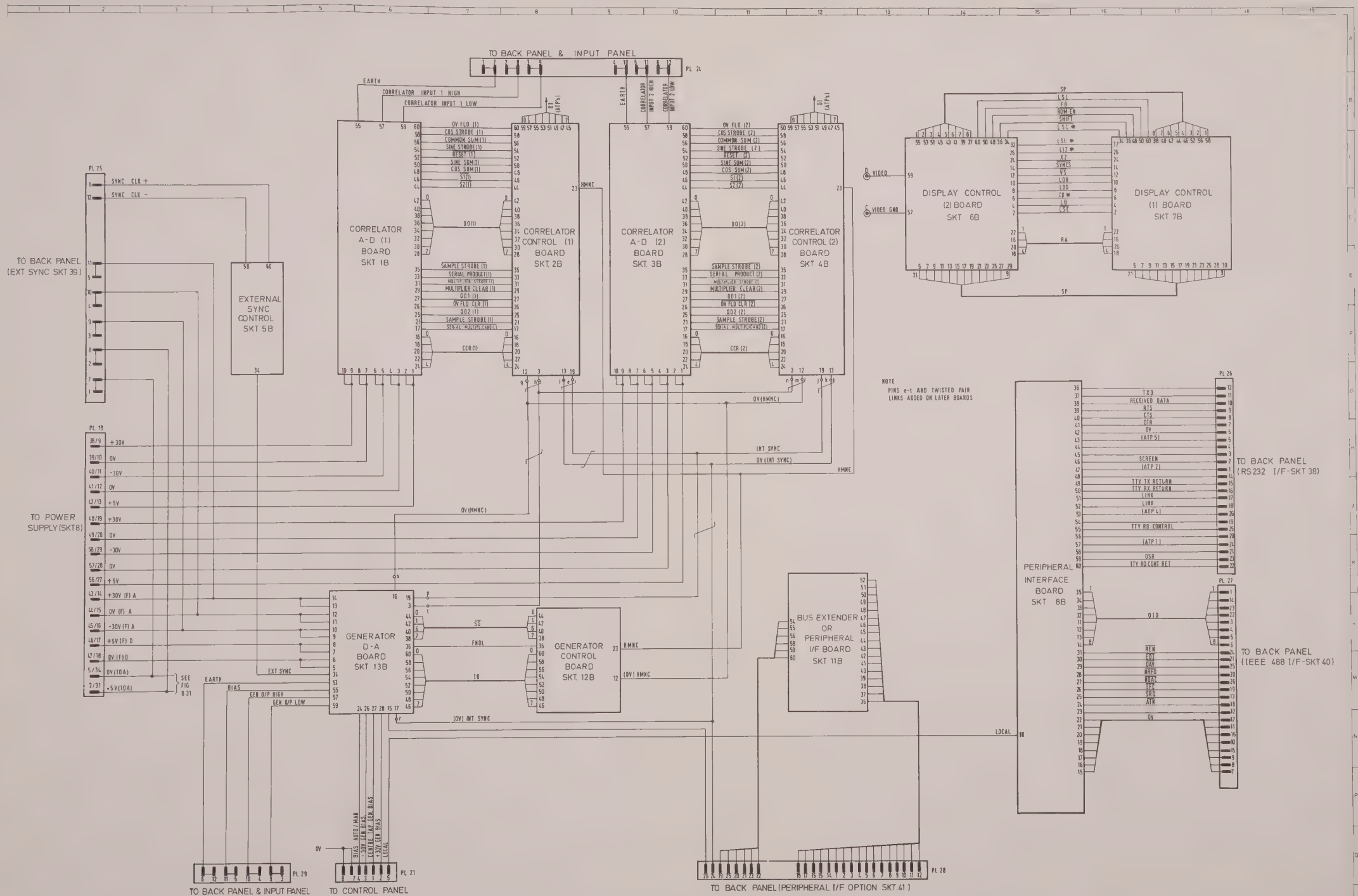
CONTAINING

BOARD	SOCKET
CORRELATOR A/B (1)	1A/B
CORRELATOR CONTROL (1)	2A/B
CORRELATOR A/B (2)	3A/B
CORRELATOR GENERATOR (2)	4A/B
EXTERNAL SYNC CONTROL	5A/B
DISPLAY CONTROL 2	6A/B
DISPLAY CONTROL 1	7A/B
PERIPHERAL INTERFACE	8A/B
PROCESSOR & CONTROL	9A
MEMORY	10A
BUS EXTENDER OR PERIPHERAL I/F	11A
GENERATOR CONTROL	12A/B
GENERATOR O/A	13A/B

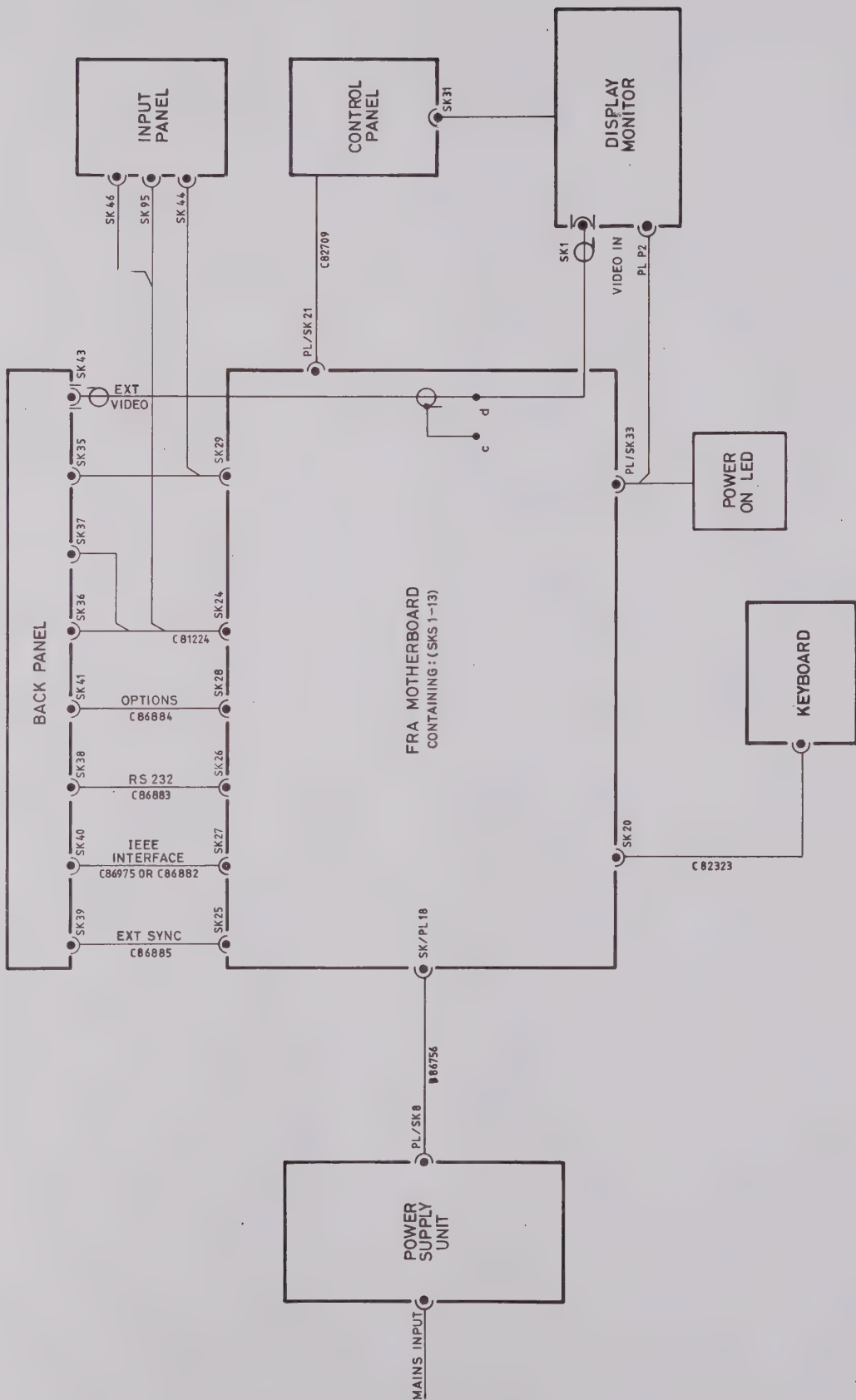
REFER TO MOTHERBOARD INTERCONNECTIONS

FREQUENCY RESPONSE ANALYSER SE2450 FIG8-30
FRA MOTHERBOARD-EXT. CONNECTIONS





FREQUENCY RESPONSE ANALYSER SE 2450
FRA MOTHERBOARD-INTERNAL BUS CONNECTIONS(SIDE B)



FREQUENCY RESPONSE ANALYSER SE2450 FIG 8.33
CABLEFORM INTERCONNECTIONS

SECTION 9

PARTS LISTS

PL No.	LIST OF CONTENTS	Page No.
	Ordering Information	9.2
	<i>Component Lists</i>	
88968	Basic FRA Assembly	9.3
82026	Processor & Cursor Control Board	9.7
82021	Memory Board	9.10
82021/02	Memory 2 Board	9.13
82001	Generator Control Board	9.15
82036/01	Generator D/A 2 Board	9.18
82036	Generator D/A Board	9.22
88610	Generator D/A Daughter Board	9.26
82006	Correlator Control Board	9.27
88602	Correlator Control Daughter Board	9.29
82041	Correlator A/D Board	9.30
82051	Display Control 1 Board	9.35
82056	Display Control 2 Board	9.37
90221	Alphanumeric Control Board	9.40
82061	FRA Motherboard	9.43
81222	Keyboard Assembly	9.44
82086	Keyboard 1 Control Logic Board	9.45
82091	Keyswitch 2 Board	9.47
81218	Keyswitch Assembly	9.48
81221	Power Supply Unit	9.49
82071	Power Supply Board 1	9.53
82076	Power Supply Board 2	9.55
82081	Power Supply Motherboard	9.59
86872	Display Monitor Module	9.61
86900	CRT POT Board	9.64
86958	CRT Earth Braid Assembly	9.65
88622	LED Cableform	9.66
86949	Input Panel	9.67
82709	Control Panel	9.68
81224	Back Panel	9.70
86883	Peripheral I/F Cableform 1	9.72
86884	Peripheral I/F Cableform 2	9.74
86882	IEEE 488 Cableform	9.76
86885	External Sync Cableform 1	9.78
86959	Accessory Kit	9.79

1. ORDERING INFORMATION

To order a replacement part, address the order to the local agent or to Service Department, SE Labs (EMI) Ltd:

Southern Area

North Feltham Trading Estate,
Spur Road,
Feltham,
Middlesex TW14 0TD

Tel No: 01 751 5951

Midland Area

Bessel Lane,
Stapleford,
Nottingham NG9 7BX

Tel No: 0602 397255

Northern Area

11 Commercial Road,
off Greaves Street,
Oldham,
Lancashire OL1 1DP

Tel No: 061 652 0073

Specify the following information for each part:

- (a) Model and serial number of the equipment
- (b) PL number
- (c) Circuit reference
- (d) SEL item number
- (e) Stock description and manufacturer's reference.

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
T01					0		ASSY DRG-E88968
001	PL/081171/00	#	CARD FRAME DETAIL ASSY	1	EA		CARD FRAME DETAIL ASSY
002	PL/081221/00	#	POWER SUPPLY	1	EA		POWER SUPPLY ASSY 230V
003	PL/086959/00	#	ACCESSORY KIT	1	EA		ACCESSORY KIT
004	PL/081222/00	#	KEYBOARD ASSY	1	EA		KEYBOARD ASSY
005	PL/081223/00	#	FRONT FRAME ASSY	1	EA		FRONT FRAME ASSY
006	PL/081224/00	#	BACK PANEL ASSY	1	EA		BACK PANEL ASSY
007	PL/081225/00	#	CHASSIS ASSY	1	EA		CHASSIS ASSY
008	PL/081226/00	#	HANDLE ASSY	1	EA		HANDLE ASSY
009	PL/082001/00	#	GEN. CONTROL PCB ASSY	1	EA		GENERATOR CONTROL PCB ASSY
010	PL/082006/00	#	CORR. CONTROL PCB ASSY	2	EA		CORRELATOR CONTROL PCB ASSY
013	PL/082026/00	#	PROCESS/CURSOR PCB ASSY	1	EA		PROCESSOR CONTROL PCB ASSY
015	PL/082036/01	#	GEN.D-A 1 PCB ASSY	1	EA		GENERATOR D/A CONTROL 1 PCB ASSY
016	PL/082041/00	#	CORRELATOR A-D PCB ASSY	2	EA		CORRELATOR A/D CONTROL PCB ASSY
018	PL/091128/00	#	EARTH LINK ASSY	1	EA		EARTH LINK ASSY
020	PL/082061/00	#	MOTHERBOARD PCB ASSY	1	EA		MOTHERBOARD ASSY
021	PL/082674/00	#	TOP COVER ASSY	1	EA		TOP COVER ASSY
022	PL/082706/00	#	BOTTOM COVER ASSY	1	EA		BOTTOM COVER ASSY
023	PL/082709/00	#	CONTROL PANEL ASSY	1	EA		CONTROL PANEL ASSY
024	PL/086756/00	#	CABLEFORM, MOTHERBOARD TO PSU	1	EA		CABLEFORM ASSY PSU TO MOTHERBOARD
025	PL/086761/00	#	CHASSIS PLATE	1	EA		CHASSIS PLATE ASSY
026	PL/086764/00	#	TOP MOUNTING STRIP ASSY	1	EA		MTG STRIP ASSY TOP
027	PL/086766/00	#	BOTTOM MOUNTING STRIP	1	EA		MTG STRIP ASSY BOTTOM
028	PL/086900/00	#	C.R.T. POT PCB ASSY	1	EA		CRT POT BOARD PCB ASSY
029	PL/086872/00	#	MONITOR MODULE ASSY	1	EA		MONITOR MODULE KIT ASSY

IT COMP.	NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
031	PL/086958/00	# C.R.T. EARTH BRAID	1	EA	CRT EARTH BRAID ASSY
036	081228/00	1 D HANDLE BEZEL MOULDING	1	EA	
038	082338/00	1 B L/H CHASSIS RUNNER	1	EA	
039	082340/00	1 B PUSH ROD CARRIER	2	EA	
040	082341/00	1 C ANGLE PLATE	1	EA	
042	082651/00	1 B PUSH ROD	1	EA	COMPONENT LABEL ASSY
043	082652/00	1 B BUSH	1	EA	
044	082653/00	1 B PUSH BUTTON BEZEL	1	EA	
045	082665/00	1 B EXTRUSION MODIFIED	4	EA	
046	PL/086984/00	# COMPONENT LABEL ASSY	1	EA	
047	082758/00	1 B R/H CHASSIS RUNNER	1	EA	IDENT STRIP ASSY
048	082761/00	1 A FOOT RETAINER	4	EA	
049	090056/00	1 A MOD STATE LABEL	1	EA	
050	082787/00	1 B CARD FRAME BRACING STRAP	2	EA	
051	086769/00	1 C L.E.D.RETAINER	1	EA	
052	086770/00	1 A SHOULDER SCREW	4	EA	
053	086785/00	1 A SPACER	2	EA	
054	086786/00	1 A SPACER,CARD FRAME	32	EA	
055	086787/00	1 A SPACER,CARD FRAME	12	EA	
056	086788/00	1 A SPACER,CARD FRAME	4	EA	
057	086789/00	1 A SPACER CARD FRAME	4	EA	
058	090983/00	1 A SPACER CRT	4	EA	
059	PL/088483/00	# IDENT STRIP ASSY	1	EA	
061	WS/060701/00	1 P.C.B CARD GUIDE 35 0456C VER0	26	EA	
062	WS/060702/00	1 RUBBER FOOT A 301 R.MOSS	4	EA	

IT COMP. NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
064	WS/060703/00	1 FOOT ADHESIVE BACK SJ 5012 3M	4	EA	LED CABLEFORM ASSY
066	PL/088622/00	# LED CABLEFORM ASSY	1	EA	
067	WS/060761/00	1 C.R.T 9WITH LUGS M23-112-GH	1	EA	
073	WS/060658/00	1 SPRING COMP1.5X7/32D LS800-19	1	EA	
074	NS/020215/00	1 CIRCLIP EXT-SER:E:DN1500 019MS	2	EA	
075	YS/040004/00	1 SC P0Z CSK M3 X 10	MSZP 7	EA	
076	YS/040001/00	1 SC P0Z CSK M3 X 5	MSZP 2	EA	
077	YS/040002/00	1 SC P0Z CSK M3 X 6	MSZP 3	EA	
078	YS/040021/00	1 SC P0Z CSK M5 X 12	MSZP 6	EA	
079	YS/040106/00	1 SC P0Z PAN M5 X 12	MSZP 4	EA	
080	YS/040086/00	1 SC P0Z PAN M3 X 6	MSZP 8	EA	
081	YS/040087/00	1 SC P0Z PAN M3 X 8	MSZP 14	EA	
082	YS/040095/00	1 SC P0Z PAN M4 X 8	MSZP 8	EA	
083	YS/040096/00	1 SC P0Z PAN M4 X 10	MSZP 4	EA	
084	YS/040097/00	1 SC P0Z PAN M4 X 12	MSZP 4	EA	
087	YS/040684/00	1 SC SKT GRUB M3 X 3 CUP	MSZP 1	EA	
089	YS/041387/00	1 SC P0Z Z PAN SLFTAP 5/16 MSCHP	4	EA	
090	YS/041540/00	1 SCR P0Z CSK SLF TAB:B:N06X3/8	8	EA	
094	YS/040385/00	1 NUT HEX FULL M3	MSZP 10	EA	
096	YS/040403/00	1 WASHER STD M5 HEAVY	MSZP 4	EA	
097	YS/040401/00	1 WASHER STD M3 HEAVY	MSZP 2	EA	
098	NS/019985/00	1 WASHER A26-3024	JERMYN 4	EA	
100	YS/040465/00	1 WASHER CRINKLE M3	ST.S 26	EA	
101	YS/040466/00	1 WASHER CRINKLE M4	ST.S 20	EA	
102	YS/040463/00	1 WASHER CRINKLE M5	BCUCP 4	EA	

IT COMP. NUMBER S STOCK DESCRIPTION										QTY	UN	NOTES
104	YS/040435/00	1	WASHER SHK/PRF M5	INT/T	MSCP	2		EA				
105	YS/040434/00	1	WASHER SHK/PRF M4	INT/T	MSCP	3		EA				
106	YS/040433/00	1	WASHER SHK/PRF M3	INT/T	MSCP	2		EA				
108	LS/017072/00	1	TY RAP TY-24M THOMAS & BETT			5		EA				

IT	COMP.	NUMBER	S	STÖCK	DESCRIPTION	QTY	UN	NOTES
T01				0				NOTE- THIS PL ASSY TÖ D82026
T02				0				CIRCUIT DIAGRAM E82025
001	PL/087592/00	#	PCB	DRILLED,PL	ONLY	1	EA	
002	QS/022599/00	1	RIVET	1/8"	AL/AL 1801-0408	4	EA	* ALTN TÖ ITEMS 9,10,11
003	082113/14	1	C	BUSBAR,14	LEGS	1	EA	
004	087880/00	1	A	INSULATOR		1	EA	FÖR ITEM 39
005	082113/04	1	C	BUSBAR,4	LEGS	1	EA	
006	082113/06	1	C	BUSBAR,6	LEGS	2	EA	
007	087918/00	1	C	LABEL	(NUMBER)	1	EA	
008	WS/060079/00	1	PCB	HANDLE	BLACK CH 10036/3	2	EA	
009	YS/040087/00	1	SC	PÖZ	PAN M3 X 8	MSZP 4	EA	SEE ITEM 2 FÖR ALTN
010	YS/040385/00	1	NUT	HEX	FULL M3	MSZP 4	EA	SEE ITEM 2 FÖR ALTN
011	YS/040461/00	1	WASHER	CRINKLE	M3	BCUCP 4	EA	SEE ITEM 2 FÖR ALTN
012	WS/060078/00	1	EJECTÖRS	WITH	PINS 13301(PAIR)	1	EA	
013	AS/001776/00	1	3	WAY	SKT BL/BL/BL 505	PCA 6X 3	EA	
014	087905/00	1	C	LABEL	(TITLE)	1	EA	
015				0				A82028,MÖD.RECORD SHT,REF.ÖNLY
016	DS/034093/00	1	R	5K62	1% 0.4W	50PPM MR25/VTM 2	EA	R12,R18.
017	DS/033876/00	1	R	1K	1% 0.4W	50PPM MR25/VTM 5	EA	R7,R8,R9,R14,R15
018	DS/034877/00	1	RES	221R	1% 0.4W	100PPM MR25 4	EA	R24-27
019	DS/034884/00	1	R	511R	1% 0.4W	50PPM MR25/VTM 1	EA	R16.
020	DS/033532/00	1	R	681R	1% 0.4W	50PPM MR25/VTM 1	EA	R17
021	DS/036111/00	1	RES	PACK	4308R-101-562	BÖURNS 1	EA	RP2
022	DS/036295/00	1	RES	PACK	5 X 5K6	4306R 101 562 1	EA	RP1
023	CS/031745/00	1	CAP	4.7	MF 25V	TAG 4.7/25	ITT 3	C6,C8,C10

PARTS LIST 082026/00 ISSUE 13 C.N. 09672 DATE 08/12/80 C>PCB ASSY,PROCESSOR BOARD/CURSÖR CÖNTRÖL SE2450										00245000002

IT	COMP.	NUMBER	S	STÖCK	DESCRIPTION	QTY	UN	NOTES		
024	CS/031749/00	1	CAP	100MF	20% 6.3V TAG 100/6.3	1	EA	C61		
026	CS/031323/00	1	CAP	VARIABLE	2-10PF 808-00005	1	EA	C3.		
027	CS/031723/00	1	CAP	0.1MFD	10% 100V 8131M100	4	EA	C7,9,11,62		
028	CS/031721/00	1	CAP	0.01MF	10% 100V 8131M100	48	EA	C12-49,C51-60		
029	DS/033528/00	1	R	332R	1% 0.4W 50PPM MR25/VTM	6	EA	R1-4,6,20		
031	BS/002045/00	1	DIÖDE	10M/A	100V 1N914 TRANSIT	1	EA	D1.		
032	QS/022736/00	1	SWITCH	ÖN/ÖFFX8	DIL 24008G WAY	1	EA	10D. (S3-S7)		
033	SS/024409/00	1	ADHESIVE	IS 415		0	BT	A/R,FÖR FIXING ITEM 4		
034	091258/00	1	A	LOCKING	RÖD	1	EA	FÖR ITEM 32		
035	KS/015700/00	1	PIN	-75401/002	BERG.	6	EA	FÖR LK1,LK2		
036	LS/017009/00	1	KINAR	INSUL	1.025MM SIN SPCW	0	M	A/R FÖR LK1,2		
038	DS/034899/00	1	RES	20K	.4W MR25 VTM/471	1	EA	R19		
039	WS/060705/00	1	CRYSTAL	18.432	MHZ MJ XTAL ELE	1	EA	XL1		
040	ÖS/020220/00	1	LACING	CÖRD	NYLÖN BLACK R88W	0	RL	60MM,FÖR SECURING ITEM 39		
041	BS/003135/00	1	DIÖDE	HÖLDER	A1136 JERMYN	1	EA	FÖR MTG.ITEM 31		
042	BS/005582/00	1	I	C SKT	40 PIN 740-AG3D AUGAT	1	EA	FÖR ITEM 106		
043	BS/005211/00	1	I/C	SKT	28PIN US-2-28-110NB	1	EA	FÖR ITEM 118		
044	BS/005014/00	1	I/C	SKT	16PIN US-2-16-110-N-B	3	EA	FÖR ITEMS 115 & 112		
045	BS/005136/00	1	I/C	SKT	24PIN US-2-24-110-N-B	1	EA	FÖR ITEM 109		
046	BS/003981/00	1	I/C	SN74LS00N	TEXAS ÖNLY	1	EA	4E		
047	BS/003284/00	1	I.C	SN	74S00/MPS 013 TEX ÖNTY	1	EA	3E		
049	BS/003982/00	1	I/C	SN74LS02N	TEXAS ÖNLY	1	EA	3C		
052	BS/003983/00	1	I/C	SN74LS04N	TEXAS ÖNLY	3	EA	3A,4D,7D		
053	BS/003277/00	1	I/C	SN74S04MPS013	TEXAS	1	EA	1A		
055	BS/003984/00	1	I/C	SN74LS08N	TEXAS ÖNLY	2	EA	2B,4B		

IT COMP. NUMBER S	STÖCK DESCRIPTION	QTY	UN	NOTES
058 BS/005486/00	1 I/C SN74S09N TEXAS ÖNLY	1	EA	4F
061 BS/005030/00	1 I/C SN74LS32N ÖPEN MARKET	1	EA	3D
064 BS/005094/00	1 I/C SN74LS37N ÖPEN MARKET	1	EA	4C
067 BS/006090/00	1 I.C SN74S132N TEXAS ÖNLY	1	EA	3F
070 BS/005242/00	1 I/C SN74LS51N TEXAS ÖNLY	1	EA	2E
073 BS/005008/00	1 I/C SN74LS74N TEXAS ÖNLY	2	EA	1D, 4A.
074 BS/005133/00	1 I/C SN74S74N ÖPEN MARKET	1	EA	1B
076 BS/005011/00	1 I/C SN74LS85N TEXAS ÖNLY	5	EA	6B, 6C, 6D, 10E, 10F
079 BS/005240/00	1 I/C SN74LS107N TEXAS ÖNLY	2	EA	2C, 2D
082 BS/003288/00	1 I/C SN74S112MPS013 TEXAS	1	EA	1F (BOUGHT TO MPS 013)
085 BS/005120/00	1 I/C SN74LS161N ÖPEN MARKET	3	EA	5B, 5C, 5D
088 BS/005788/00	1 I.C SN 74LS195 TEXAS ÖNLY	1	EA	2A
091 BS/005509/00	1 I/C SN74S258N TEXAS ÖNLY	4	EA	8C, 8D, 9E, 9F
094 BS/005301/00	1 I/C SN74278N TEXAS ÖNLY	1	EA	3B
097 BS/005227/00	1 I/C SN74S412 TEXAS ÖNLY	3	EA	6A, 8A, 10C
100 BS/005156/00	1 I/C SN74LS42AN ÖPEN MARKET	1	EA	7B
106 BS/005750/00	1 I.C P 8080 A INTEL ÖNLY	1	EA	9B
109 BS/005746/00	1 I.C P 8214 INTEL ÖNLY	1	EA	5F
112 BS/005233/00	1 I/C P8216 INTEL ÖNLY	2	EA	7F, 8F
115 BS/006081/00	1 I.C CLOCK GEN D8224 INTEL ÖNLY	1	EA	8B
118 BS/005747/00	1 I.C P 8228 INTEL ÖNLY	1	EA	10A

IT COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
030	BS/005228/00	1	I/C SN74S157N TEXAS ONLY	2	EA	9A, 9B.
031	BS/005227/00	1	I/C SN74S412 TEXAS ONLY	2	EA	10A, 10B.
040	BS/005014/00	1	I/C SKT 16PIN US-2-16-110-N-B	16	EA	FOR MTG ITEM 86
041	BS/005136/00	1	I/C SKT 24PIN US-2-24-110-N-B	10	EA	FOR MTG ITEMS 31, 77-84
043	LS/017534/00	1	PVC EXTRUSION. CS20 PLASTICABL	0	M	85MM
044	SS/024409/00	1	ADHESIVE IS 415	0	BT	A/R
046	DS/036294/00	1	RES PACK 9X180R 2% 4310R-101-	1	EA	RP1
047	DS/036293/00	1	RES PACK 9X270R 2% 4310R-101-	1	EA	RP2
048	DS/036334/00	1	RES PACK 7<180R 4308R-101-181	1	EA	RP3 (FOR ALTN, SEE ITEM 50)
049	DS/036115/00	1	RES PACK 4308R-101-271 BOURNS	1	EA	RP4
050	DS/036347/00	1	RES PACK 7X180R 764-1-R-180 BK	0	EA	* ALTN TO ITEM 48
052	DS/034433/00	1	R 182R 1% 0.4W 50PPM MR25/VTM	5	EA	R8, 9, 20, 22, 24.
053	DS/034877/00	1	RES 221R 1% 0.4W 100PPM MR25	3	EA	R14, 16, 18.
054	DS/034879/00	1	RES 274R 1% 0.4W 100PPM MR25	5	EA	R10, 11, 21, 23, 25
055	DS/033528/00	1	R 332R 1% 0.4W 50PPM MR25/VTM	5	EA	R6, 7, 15, 17, 19.
057	DS/033876/00	1	R 1K 1% 0.4W 50PPM MR25/VTM	2	EA	R4, 5
058	DS/033538/00	1	R 2K21 1% 0.4W 50PPM MR25/VTM	1	EA	R3
059	DS/034410/00	1	R 3K92 1% 0.4W 50PPM MR25/VTM	2	EA	R1, 2.
061	CS/031745/00	1	CAP 4.7 MF 25V TAG 4.7/25 ITT	3	EA	C1, C3, C5,
063	CS/031723/00	1	CAP 0.1MFD 10% 100V 8131M100	5	EA	C2, 4, 6, 7, 8.
065	CS/031721/00	1	CAP 0.01MF 10% 100V 8131M100	71	EA	C9-C79 INC.
068	BS/002873/00	1	TRANSISTOR 2N5415 RCA	1	EA	TR1
070	BS/002263/00	1	MOUNTING PAD T05-001 JERMYN	1	EA	FOR MTG ITEM 68
077	087891/00	1	A I/C PROGRAM FROM BS5800	1	EA	IC11B
078	087892/00	1	A I/C PROGRAM FROM BS5800	1	EA	IC11A

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
079	087893/00	1	A I/C PRGRMD FROM BS5800	1	EA	IC12B
080	087894/00	1	A I/C PRGRMD FROM BS5800	1	EA	IC12A
081	087895/00	1	A I/C PRGRMD FROM BS5800	1	EA	IC13B
082	087896/00	1	A I/C PRGRMD FROM BS5800	1	EA	IC13A
083	087897/00	1	A I/C PRGRMD FROM BS5800	1	EA	IC14B
084	087898/00	1	A I/C PRGRMD FROM BS5800	1	EA	IC14A
086	BS/005013/00	1	I/C MK4027-3 MOSTEK ONLY	16	EA	FOR CIRCUIT NOS, SEE ITEMS 900, 901
900				0		1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 6A, 6B,
901				0		7A, 7B, 8A, 8B

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
T01	052021/02	4	D	ASSY DRG	0	EA	REF. ONLY
T02	090917/00	4	E	CCT DIAG	0	EA	REF. ONLY
001	090918/00	4	A	MOD.RECORD SHEET	0	EA	REF. ONLY
002	PL/090927/00	1	PCB DRILLED	PL ONLY	1	EA	
003	087919/00	1	C	PCB LABEL	1	EA	
004	088916/00	1	B	TITLE LABEL	1	EA	
005	WS/060079/00	1	PCB HANDLE	BLACK CH 10036/3	2	EA	
006	YS/040087/00	1	SC P02	PAN M3 X 8	MSZP 4	EA	
007	YS/040385/00	1	NUT	HEX FULL M3	MSZP 4	EA	
008	YS/040461/00	1	WASHER	CRINKLE M3	BCUCP 4	EA	
009	WS/060078/00	1	EJECTORS	WITH PINS 13301 (PAIR)	1	EA	
010	AS/001776/00	1	3 WAY SKT	BL/BL 505 PCA 0X	2	EA	
011	KS/015700/00	1	PIN	-75401/002 BERG.	7	EA	TP1 TO TP6 INCL.
012	LS/017068/00	1	CABLE CO-AX	R61703U RADIAL	0	M	170MM LONG
013	SS/024601/00	1	SEALANT	RTV CLEAR 3145 DOW COR	0	TB	TO SECURE ITEM 12 A/R
014	BS/005014/00	1	I/C SKT	16PIN US-2-16-110-N-B	36	EA	FOR MT6 ITEMS 59,71,72,73
015	BS/005136/00	1	I/C SKT	24PIN US-2-24-110-N-B	12	EA	FOR MT6 ITEMS 60 TO 70 INCL.
019	091086/00	4	A	ASSY STATE RECORD SHEET	0	EA	REF. ONLY
020	DS/034433/00	1	R 182R	1% 0.4W S0PPH MR25/VTM	3	EA	R7,8,10
021	DS/034879/00	1	RES	274R 1% 0.4W 100PPH MR25	3	EA	R9,11,6
022	DS/033876/00	1	R 1K	1% 0.4W S0PPH MR25/VTM	2	EA	R4,5,
023	DS/033538/00	1	R 2K21	1% 0.4W S0PPH MR25/VTM	1	EA	R3
024	DS/034410/00	1	R 3K92	1% 0.4W S0PPH MR25/VTM	2	EA	R1,2
029	DS/036294/00	1	RES	PACK 9X180R 2% 4310R-101-	2	EA	RP4,6
030	DS/036293/00	1	RES	PACK 9X270R 2% 4310R-101-	2	EA	RP3,5

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
031	DS/036334/00 1 RES PACK 7<180R 4308R-101-181	1	EA	RP2
032	DS/036115/00 1 RES PACK 4308R-101-271 BOURNS	1	EA	RP1
033	DS/036375/00 1 RES PK 783-5-220(R1)/330(R2)	1	EA	RP7
034	DS/036419/00 1 RES PACK 8-3K3 L09-1-R3.3K BEK	1	EA	RP8
039	CS/031723/00 1 CAP 0.1NFD 10% 100V 8131M100	36	EA	C2,4,6 TO 39 INCL
040	CS/030991/00 1 CAP 10NF -20<50% 16V TA610/16	6	EA	C40 TO 45 INCL
041	WS/060856/00 1 CAP BUSBAR 8-PAC/8V-3/17.5.1.3	2	EA	
042	WS/060855/00 1 CAP BUSBAR 8-PAC/8V2/17.5.3	2	EA	
043	WS/060854/00 1 CAP BUSBAR 8-PAC 8V2/12.8.6	1	EA	
045	CS/031718/00 1 CAP 47NF 20% 16V TAG 47/16 ITT	3	EA	C1,3,5
047	BS/002873/00 1 TRANSISTOR 2N5415 RCA	1	EA	TR1
052	BS/003981/00 1 I/C 8N74LS00N TEXAS ONLY	2	EA	60,40
053	BS/003982/00 1 I/C 8N74LS02N TEXAS ONLY	1	EA	30,
054	BS/003983/00 1 I/C 8N74LS04N TEXAS ONLY	3	EA	160,170,180
055	BS/007406/00 1 I/C 8N7406N OPEN MARKET	1	EA	10
056	BS/003984/00 1 I/C 8N74LS02N TEXAS ONLY	1	EA	90
057	BS/003985/00 1 I/C 8N74LS14N TEXAS ONLY	1	EA	100
058	BS/005008/00 1 I/C 8N74LS74N TEXAS ONLY	1	EA	70
059	BS/005228/00 1 I/C 8N74S157N TEXAS ONLY	2	EA	17A,17B
060	BS/005227/00 1 I/C 8N74S412 TEXAS ONLY	2	EA	3C,1C
071	090920/00 1 C I/C PROGRAM FROM BS5513	1	EA	130
072	090921/00 1 C I/C PROGRAM FROM BS5513	1	EA	15C
073	BS/005013/00 1 I/C 8N4027-3 MOSTEK ONLY	32	EA	1A TO 16A INCL, 1B TO 168 INCL
080	LS/016017/00 1 WIRE.5K6 RL 22SW6	0	KG	FOR LK1 A/R
081	BS/002263/00 1 MOUNTING PAD T05-001 JERMYN	1	EA	FOR MT6 ITEM 47

PARTS LIST 082001/00 ISSUE 09 C.N. 09691 DATE 05/12/80 C>PCB ASSY, GENERATOR CONTROL SE2450							0024500000	

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY	UN	NOTES
T01						0		THIS PL ASSY TO D82001
T02						0		CIRCUIT DIAGRAM E82000
001	PL/087604/00	#	PCB	DRILLED, PL ONLY		1	EA	
007	087921/00	1	C	LABEL (NUMBER)		1	EA	
008	WS/060079/00	1	PCB	HANDLE BLACK CH 10036/3		2	EA	
009	YS/040087/00	1	SC	P0Z PAN M3 X 8	MSZP	4	EA	SEE ITEM 16 FOR ALTN
010	YS/040385/00	1	NUT	HEX FULL M3	MSZP	4	EA	SEE ITEM 16 FOR ALTN
011	YS/040461/00	1	WASHER	CRINKLE M3	BCUCP	4	EA	SEE ITEM 16 FOR ALTN
012	WS/060078/00	1	EJECTORS	WITH PINS 13301(PAIR)		1	EA	
013	AS/001776/00	1	3	WAY SKT BL/BL/BL 505 PCA 0X		2	EA	
014	087908/00	1	C	LABEL (TITLE)		1	EA	
015						0		A REF MOD RECORD SHEET 82003
016	QS/022599/00	1	RIVET	1/8" AL/AL 1801-0408 AVD		4	EA	* ALTN TO ITEMS 9,10,11
017	DS/034638/00	1	RES	20R0 5% 2.5W W21 WELWYN		1	EA	R24
018	DS/033876/00	1	R	1K 1% 0.4W 50PPM MR25/VTM		10	EA	R8,15-23
019	DS/034885/00	1	R	562R 1% 0.4W 50PPM MR25/VTM		2	EA	R10,R11,
020	DS/034093/00	1	R	5K62 1% 0.4W 50PPM MR25/VTM		1	EA	R5
021	DS/033528/00	1	R	332R 1% 0.4W 50PPM MR25/VTM		5	EA	R1,R3,R7,R13,R14
023	DS/033532/00	1	R	681R 1% 0.4W 50PPM MR25/VTM		1	EA	R9,
025	DS/036111/00	1	RES	PACK 4308R-101-562 BOURNS		1	EA	RP1
029	CS/031737/00	1	CAP	470PF 2.5% 30V HS SUFLEX		4	EA	C38 TO 41
030	CS/031659/00	1	CAP	47MF 20% 16V TAG47/16 ITT		1	EA	C36
031	CS/031731/00	1	CAP	47PF 2.5% 30V HS SUFLEX		1	EA	C1
032	CS/031729/00	1	CAP	33PF 2.5% 63V HS SUFLEX		1	EA	C2
033	CS/030537/00	1	CAP	0.047MFD 20% 250V MULLARD		1	EA	C3
A REF MOD RECORD SHEET 82003								

9.15

IT COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
034	CS/032734/00	1	CAP 3.3 MF 20% 63V MKB3 WAYCOM	1	EA	C4
035	CS/031745/00	1	CAP 4.7 MF 25V TAG 4.7/25 ITT	3	EA	C7, 9, 35
036	CS/031723/00	1	CAP 0.1MFD 10% 100V 8131M100	2	EA	C6, C8
037	CS/031721/00	1	CAP 0.01MF 10% 100V 8131M100	23	EA	C10-23, 25-33.
038	CS/032342/00	1	CAP 10PF <-1PF 30V HS10/1-7/30	1	EA	C24
039	CS/031038/00	1	CAP 1MF 20% 35V TAG1.0/35 ITT	1	EA	C34
040	CS/032254/00	1	CAP 22PF 2.5% 30V HS30 SUFLEX	1	EA	C37
041	BS/003180/00	1	Z/DIODE 7VS 5% 1W BZX61C7V5	1	EA	D1
042	BS/003342/00	1	TRANSISTOR TYPE BC182 TEXAS	1	EA	TR1
043	BS/005906/00	1	VOLT REG <5V 200MA LM109H	1	EA	REG 1
044	BS/002968/00	1	MOUNTING PAD T05/18/002 JERMYN	1	EA	FOR ITEM 42
045	BS/003135/00	1	DIODE HOLDER A1136 JERMYN	9	EA	FOR ITEMS 29, 31, 32, 38, 40, 41
046	BS/003981/00	1	I/C SN74LS00N TEXAS ONLY	1	EA	8A
049	BS/003983/00	1	I/C SN74LS04N TEXAS ONLY	1	EA	10A
052	BS/005589/00	1	I/C SN74LS10N TEXAS ONLY	1	EA	4B
055	BS/005352/00	1	I/C SN74LS42N TEXAS ONLY	1	EA	9C
058	BS/005011/00	1	I/C SN74LS85N TEXAS ONLY	2	EA	2A, 2B.
064	BS/003242/00	1	IC TYPE SN74121N/MPS013 TEXAS	1	EA	6A
067	BS/005292/00	1	I/C SN74S124N TEXAS ONLY	2	EA	4A, 2C
070	BS/005789/00	1	I.C SN 74150N TEXAS ONLY	2	EA	11C, 13C
071	BS/003832/00	1	I.C. SN74S132 OPEN MARKET	1	EA	9A
073	BS/005721/00	1	I.C 74LS174 S.E.L DRG A97009	2	EA	10B, 11B
076	BS/005516/00	1	I/C SN74LS163N TEXAS ONLY	5	EA	8B, 5B, 6B, 7B, 9B.
079	BS/005787/00	1	I.C SN 74LS197N TEXAS ONLY	7	EA	11A, 12A, 12B, 13A, 13B, 14A, 14B,
082	BS/005227/00	1	I/C SN74S412 TEXAS ONLY	3	EA	3C, 5C, 7C

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
085 BS/005786/00	1 I.C SN 74LS196N TEXAS ONLY	4	EA	1A,1B,1C,1D,
088 BS/003146/00	1 I/C MC4044P MOTOROLA ONLY	1	EA	5A
091 QS/022736/00	1 SWITCH ON/OFFX8 DIL 24008G WAY	1	EA	S1-S8.
092 091258/00	1 A LOCKING ROD	1	EA	FOR USE WITH ITEM 91
093 BS/005014/00	1 I/C SKT 16PIN US-2-16-110-N-B	2	EA	FOR MTG IC2C,4A
094 082113/10	1 C BUSBAR 10 LEGS	1	EA	
095 082113/14	1 C BUSBAR, 14 LEGS	2	EA	
097 WS/060715/00	1 CRYSTAL-WIRE LEADS 10.24MHZ MJ	1	EA	XL 1
099 OS/020220/00	1 LACING CORD NYLON BLACK R88W	0	RL	A/R
105 KS/015700/00	1 PIN -75401/002 BERG.	3	EA	FOR LK1
107 LS/017009/00	1 KINAR INSUL 1.025MM SIN SPCW	0	M	A/R FOR LK1

PARTS LIST 082036/01 ISSUE 01 C.N. 09452 DATE 21/05/80 C>PCB ASSY GENERATOR D/A 1 SE2450 3031040001									

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES		
T01					0		ASSY DRG-D82036/01		
T02					0		CCT DIAG-E88662		
001	PL/088667/00				1		PCB DRILLED		
006					0		A88663,ASSY STATE RECORD SHT,REF.		
007	087922/00	C	PCB LABEL		1	EA			
008	WS/060079/00	PCB HANDLE BLACK CH 10036/3			2	EA			
009	YS/040087/00	SC P0Z PAN M3 X 8	MSZP		4	EA			
010	YS/040385/00	NUT HEX FULL M3	MSZP		6	EA			
011	YS/040461/00	WASHER CRINKLE M3	BCUCP		6	EA			
012	WS/060078/00	EJECTORS WITH PINS 13301(PAIR)			1	EA			
013	AS/001776/00	3 WAY SKT BL/BL/BL 505 PCA 0X			1	EA			
014	087910/00	C PCB LABEL			1	EA			
015					0		A88664,REF.ONLY,M0D RECORD SHT		
016	DS/036307/00	RES 6R2 5% 1W G.B AL-BRAD			2	EA	R17,18		
018	DS/036318/00	RES 200R 0.1% 25PPM RC55 RES0L			1	EA	R9		
020	DS/036319/00	RES 1K8 0.1% 25PPM RC55 RES0LU			1	EA	R8		
022	DS/033529/00	R 475R 1% 0.4W 50PPM MR25/VTM			3	EA	R1,3,19		
024	DS/036072/00	R 1K 0.05% 1/4W 15PPM RC65			1	EA	R14		
025	DS/036324/00	RES 18K 0.1% 25PPM RC55 RES0LU			1	EA	R7		
026	DS/036320/00	RES 2K21 0.5% 25PPM RC55 RES0L			1	EA	R13		
028	DS/036321/00	RES 3K32 0.5% 25PPM RC55 RES0L			3	EA	R11,16,28		
030	DS/036323/00	RES 4K02 0.5% 25PPM RC55 RES0L			1	EA	R12		
032	DS/033539/00	R 5K11 1% 0.4W 50PPM MR25/VTM			1	EA	R22		
034	DS/034060/00	RES 12K1 1% .4W MR25 VTM/471			1	EA	R23		
036	DS/036326/00	RES 360K 0.5% 25PPM RC55 RES0L			1	EA	R15		

IT COMP. NUMBER S STOCK DESCRIPTION						QTY	UN	NOTES
038	DS/034906/00	R 61K9 1% 0.4W 50PPM MR25/VTM	2	EA			R21, 24	
040	DS/034095/00	R 10K 1% 0.4W 50PPM MR25/VTM	7	EA			R2, 4, 5, 6, 20, 27, 32	
041	DS/034428/00	R 2K74 1% 0.4W 50PPM MR25/VTM	1	EA			R29-31	
042	DS/033534/00	R 825R 1% 0.4W 50PPM MR25/VTM	2	EA			R25, 26	
044	DS/036302/00	RES PACK 5X 470 4300R-101-471	7	EA			RP1-7	
046	DS/036297/00	RES PACK 9 X 10K 4310R-101-103	2	EA			RP8, 9	
049	DS/036305/00	RES PACK 5 X 10K 4306R-101-103	2	EA			RP10, 11	
052	FS/010822/00	POT 500R CERMET TRIM 0.5W 10%	1	EA			RV3	
054	FS/010583/00	POT 10K OHMS 81E/10K MORGANITE	1	EA			RV2, 4	
056	FS/010744/00	POT 20K 10% 1/2W 81E/20 A.BRAD	1	EA			RV1	
059	DS/036322/00	RES 8K25 0.5% 25PPM RC55 RESOL	1	EA			R10	
061	CS/030538/00	CAP 33PF 5% 30V HS SUFLEX	2	EA			C1, 5	
063	CS/031449/00	CAP 100PF 10% 100V ERIE	6	EA			C4, 8, 65-68	
064	CS/031498/00	CAP 1000PF 10% 100V 8131 U2J	1	EA			C56	
065	CS/031721/00	CAP 0.01MF 10% 100V 8131M100	29	EA			FOR CIRC.REFS, SEE ITEMS 900 & 901	
067	CS/031723/00	CAP 0.1MFD 10% 100V 8131M100	18	EA			FOR CIRC.REFS, SEE ITEMS 902 & 903	
069	CS/031745/00	CAP 4.7 MF 25V TAG 4.7/25 ITT	4	EA			C21, 25, 29, 30	
070	CS/031495/00	CAP 4.7MFD 10% 35V TAG4.7/35	2	EA			C3, 27	
071	CS/004912/00	47MFD 150-1.0% 40V 016/17479	2	EA			C10, 12	
074	BS/003179/00	Z DIODE 15V 5% 1W BZX.61 C.15	2	EA			D1, 2	
076	BS/003981/00	I/C SN74LS00N TEXAS ONLY	1	EA			9D	
079	BS/003983/00	I/C SN74LS04N TEXAS ONLY	1	EA			9E	
082	BS/005008/00	I/C SN74LS74N TEXAS ONLY	3	EA			10A, 11E, 12E	
085	BS/005011/00	I/C SN74LS85N TEXAS ONLY	1	EA			10B, 11B	
088	BS/003987/00	I/C SN74LS86N TEXAS ONLY	2	EA			10C	

IT COMP.	NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
091	BS/005120/00	I/C SN74LS161N OPEN MARKET	3	EA	10D,11C,11D
094	BS/005001/00	I/C SN74LS273N TEXAS ONLY	1	EA	8D
095	HS/012225/00	RELAY 181C-2 ASTRALUX	1	EA	RLA
096	BS/003526/00	I.C. LM 741CN NAT SEM ONLY	1	EA	1E
097	BS/005227/00	I/C SN74S412 TEXAS ONLY	5	EA	1A,4A,6A,7C,8A
100	088477/00	I/C SN74S471N PROGRAMMED	1	EA	9C MAKE FROM BS5234
103	BS/005328/00	I/C IL100 LITRONIX ONLY	4	EA	6E,7E,8E,10E
109	BS/005766/00	I.C HA1-2625-5 HARRIS ONLY	1	EA	1D
112	BS/005767/00	I.C HA2-2645-5 HARRIS ONLY	1	EA	2D
114	BS/005795/00	I.C BB 3571 BURR BROWN ONLY	1	EA	6D
116	BS/005799/00	I.C DAC 05 EX2 PRECISION MONO	1	EA	6C
117	BS/005792/00	I.C DAC-03-ADX1 PREC MONO ONLY	1	EA	4C
118	BS/005794/00	I.C DAC02CCX2 PRECIS MONO ONLY	1	EA	7D
121	BS/005769/00	I.C 1LQ 74 LITRONIX ONLY	8	EA	1B-8B
124	BS/003135/00	DIODE HOLDER A1136 JERMYN	6	EA	FOR MTG ITEMS 61,74,146
127	BS/005773/00	I.C SKT 18 PIN US-2-18-110-N-B	3	EA	FOR MTG ITEMS 116,117,118
128	BS/005774/00	I.C SKT 20 PIN US-2-20-110-N-B	1	EA	FOR MTG ITEM 100
129	087929/00	A HEATSINK MODIFIED	1	EA	FOR MTG ITEM 115
131	BS/005062/00	TRANSISTOR MTG PAD MON8/LF	1	EA	FOR MTG ITEM 112
132	KS/015040/00	MOUNTING 4BA CLX1/4 R4081ROUND	2	EA	FOR MTG ITEM 129
133	YS/040218/00	SC P0Z PAN M3X20 MSCHP	2	EA	FOR MTG ITEM 129
134	BS/003426/00	MOUNTING BUSH A22-2001 JERMYN	2	EA	FOR MTG ITEM 129
136	CS/032739/00	CAP 20000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T.
137	CS/032740/00	CAP 22000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T.
138	CS/032741/00	CAP 27000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T.

IT COMP. NUMBER S STOCK DESCRIPTION						QTY	UN	NOTES
39	CS/032742/00	CAP 33000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T.			
42	KS/015700/00	PIN -75401/002 BERG.	4	EA	FØR MTG C52 & LK5			
44	LS/016017/00	WIRE.5KG RL 22SWG	0	KG	A/R FØR LK1 TØ 5			
45	DS/035766/00	RES 2K49 1% 0.4W 50PPM MR25	2	EA	R33,34			
46	BS/002543/00	Z.DIODE 4.7V 5% 400M/W BZY88	2	EA	D3,4			
50	SS/024248/00	HEATSINK COMPOUND DP2623	0	EA	A/R			
52	BS/005765/00	I.C HI1-201-5 HARRIS ONLY	1	EA	1C			
900			0		C9,11,22,26,32-37,54,39-42,44-51,55,			
901			0		C69-72			
902			0		C2,3,6,7,13,14,15,16,17,18,19,20,24,			
903			0		31,38,43,53,73			

PARTS LIST 082036/00 ISSUE 10 C.N. 09507 DATE 03/07/80 C>PCB ASSY, GENERATOR D/A SE2450										00245000005

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY	UN	NOTES		
T01						0		CIRCUIT DIAGRAM NO E82035		
001	PL/087650/00					1				
007	087922/00	1	C	PCB	LABEL	1	EA			
008	WS/060079/00	1	PCB	HANDLE	BLACK CH 10036/3	2	EA			
009	YS/040087/00	1	SC	POZ	PAN M3 X 8 MSZP	4	EA	SEE ITEM 17 FOR ALTN		
010	YS/040385/00	1	NUT	HEX	FULL M3 MSZP	6	EA	SEE ITEM 17 FOR ALTN (4 OFF ONLY)		
011	YS/040461/00	1	WASHER	CRINKLE	M3 BCUCP	6	EA	SEE ITEM 17 FOR ALTN (4 OFF ONLY)		
012	WS/060078/00	1	EJECTORS	WITH	PINS 13301(PAIR)	1	EA			
014	087909/00	1	C	PCB	LABEL	1	EA			
015						0		A82038 REF MOD RECORD SHEET		
016	DS/036307/00	1	RES	6R2	5% 1W G.B AL-BRAD	2	EA	R17,R18		
017	QS/022599/00	1	RIVET	1/8"	AL/AL 1801-0408 AVD	4	EA	* ALTN TO ITEMS 9,10,11		
018	DS/036318/00	1	RES	200R	0.1% 25PPM RC55 RESOL	1	EA	R9		
020	DS/036319/00	1	RES	1K8	0.1% 25PPM RC55 RESOLU	1	EA	R8		
022	DS/033529/00	1	R	475R	1% 0.4W 50PPM MR25/VTM	4	EA	R1,3,19,33		
024	DS/036072/00	1	R	1K	0.05% 1/4W 15PPM RC65	1	EA	R14		
025	DS/036324/00	1	RES	18K	0.1% 25PPM RC55 RESOLU	1	EA	R7		
026	DS/036320/00	1	RES	2K21	0.5% 25PPM RC55 RESOL	1	EA	R13		
028	DS/036321/00	1	RES	3K32	0.5% 25PPM RC55 RESOL	3	EA	R11,R16,R28		
030	DS/036323/00	1	RES	4K02	0.5% 25PPM RC55 RESOL	1	EA	R12		
032	DS/033539/00	1	R	5K11	1% 0.4W 50PPM MR25/VTM	1	EA	R22		
034	DS/034060/00	1	RES	12K1	1% .4W MR25 VTM/471	1	EA	R23		
036	DS/036326/00	1	RES	360K	0.5% 25PPM RC55 RESOL	1	EA	R15		
038	DS/034906/00	1	R	61K9	1% 0.4W 50PPM MR25/VTM	2	EA	R21,R24		
040	DS/034095/00	1	R	10K	1% 0.4W 50PPM MR25/VTM	7	EA	R2,4,5,6,20,27,32		

PARTS LIST 082036/00 ISSUE 10 C.N. 09507 DATE 03/07/80 C>PCB ASSY, GENERATOR D/A SE2450 00245000005						

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN
NOTES						
041	DS/034428/00	1	R	2K74 1% 0.4W 50PPM MR25/VTM	1	EA
042	DS/033534/00	1	R	825R 1% 0.4W 50PPM MR25/VTM	2	EA
044	DS/036302/00	1	RES	PACK 5X 470 4300R-101-471	7	EA
046	DS/036297/00	1	RES	PACK 9 X 10K 4310R-101-103	2	EA
049	DS/036305/00	1	RES	PACK 5 X 10K 4306R-101-103	2	EA
052	FS/010822/00	1	POT	500R CERMET TRIM 0.5W 10%	1	EA
054	FS/010583/00	1	POT	10K OHMS 81E/10K MORGANITE	1	EA
056	FS/010744/00	1	POT	20K 10% 1/2W 81E/20 A.BRAD	1	EA
059	DS/036322/00	1	RES	8K25 0.5% 25PPM RC55 RESOL	1	EA
061	CS/030538/00	1	CAP	33PF 5% 30V HS SUFLEX	2	EA
063	CS/031449/00	1	CAP	100PF 10% 100V ERIE	6	EA
064	CS/031498/00	1	CAP	1000PF 10% 100V 8131 U2J	1	EA
065	CS/031721/00	1	CAP	0.01MF 10% 100V 8131M100	22	EA
067	CS/031723/00	1	CAP	0.1MFD 10% 100V 8131M100	17	EA
069	CS/031745/00	1	CAP	4.7 MF 25V TAG 4.7/25 ITT	4	EA
070	CS/031495/00	1	CAP	4.7MFD 10% 35V TAG4.7/35	2	EA
071	CS/004912/00	1	47MFD	150-1.0% 40V 016/17479	2	EA
074	BS/003179/00	1	Z	DIODE 15V 5% 1W BZX.61 C.15	2	EA
076	BS/003981/00	1	I/C	SN74LS00N TEXAS ONLY	1	EA
079	BS/003983/00	1	I/C	SN74LS04N TEXAS ONLY	1	EA
082	BS/005008/00	1	I/C	SN74LS74N TEXAS ONLY	3	EA
085	BS/005011/00	1	I/C	SN74LS85N TEXAS ONLY	1	EA
088	BS/003987/00	1	I/C	SN74LS86N TEXAS ONLY	2	EA
091	PL/088610/00				1	
094	BS/005001/00	1	I/C	SN74LS273N TEXAS ONLY	1	EA

DAUGHTER BOARD ASSY

7D

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
097	BS/005227/00 1 I/C SN74S412 TEXAS ONLY	5	EA	1A, 4A, 6A, 7C, 8A
100	088477/00 1 I/C SN74S471N PROGRAMMED	1	EA	9C MAKE FROM BS5234
103	BS/005328/00 1 I/C IL100 LITRONIX ONLY	4	EA	6E, 7E, 8E, 11A
109	BS/005766/00 1 I.C HA1-2625-5 HARRIS ONLY	1	EA	4D
112	BS/005767/00 1 I.C HA2-2645-5 HARRIS ONLY	1	EA	3E
115	BS/005795/00 1 I.C BB 3571 BURR BROWN ONLY	1	EA	1D
116	BS/005799/00 1 I.C DAC 05 EX2 PRECISION MONO	1	EA	5C
117	BS/005792/00 1 I.C DAC-03-ADX1 PREC MONO ONLY	1	EA	3C
118	BS/005794/00 1 I.C DAC02CCX2 PRECIS MONO ONLY	1	EA	6D
121	BS/005769/00 1 I.C 1LQ 74 LITRONIX ONLY	8	EA	1B, 2B, 3B, 4B, 5B, 6B, 7B, 9B
124	BS/003135/00 1 DIODE HOLDER A1136 JERMYN	4	EA	FOR MTG ITEMS 74 & 61
127	BS/005773/00 1 I.C SKT 18 PIN US-2-18-110-N-B	3	EA	FOR MTG ITEMS 117, 116, 118
128	BS/005774/00 1 I.C SKT 20 PIN US-2-20-110-N-B	1	EA	FOR MTG ITEM 100
129	087929/00 1 A HEATSINK MODIFIED	1	EA	FOR MTG ITEM 115
131	BS/005062/00 1 TRANSISTOR MTG PAD MON8/LF	1	EA	FOR MTG ITEM 112
132	KS/015040/00 1 MOUNTING 4BA CLX1/4 R4081ROUND	2	EA	TO MOUNT ITEM 129
133	YS/040218/00 1 SC P0Z PAN M3X20 MSCHP	2	EA	TO MOUNT ITEM 129
134	BS/003426/00 1 MOUNTING BUSH A22-2001 JERMYN	2	EA	TO MOUNT ITEM 129
136	CS/032739/00 1 CAP 20000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T
137	CS/032740/00 1 CAP 22000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T
138	CS/032741/00 1 CAP 27000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T
139	CS/032742/00 1 CAP 33000PF 63V 2.5% HS SUFLEX	1	EA	C52 S.O.T
142	KS/015700/00 1 PIN -75401/002 BERG.	2	EA	FOR MTG C52
144	LS/017009/00 1 KINAR INSUL 1.025MM SIN SPCW	0	M	A/R
152	BS/005765/00 1 I.C HI1-201-5 HARRIS ONLY	1	EA	2C

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
900		0		C9, 11, 22, 26, 28, 32, 33, 34, 35, 36, 37, 54,
901		0		39, 40, 41, 44, 45, 48, 49, 50, 51, 55
902		0		C2, 3, 6, 7, 13, 14, 15, 16, 17, 18, 19, 20, 24
903		0		31, 43, 38, 53

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01		0		ASSY DRG- B88610
001	PL/088612/00	1		PCB DRILLED
002	KS/015755/00	17	EA	
003	CS/031721/00	3	EA	C42,46,47
004	BS/005120/00	3	EA	10D,11C,11D

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
T01					0		NOTE- THIS PL ASSY TO
T02					0		CIRCUIT DIAGRAM E82005
001	PL/087614/00	#	PCB	DRILLED,CORR.CONTROL	1	EA	
007	087914/00	1	C	PCB LABEL	1	EA	
008	WS/060079/00	1	PCB	HANDLE BLACK CH 10036/3	2	EA	
009	YS/040087/00	1	SC	P0Z PAN M3 X 8 MSZP	4	EA	SEE ITEM 17 FOR ALTN
010	YS/040385/00	1	NUT	HEX FULL M3 MSZP	4	EA	SEE ITEM 17 FOR ALTN
011	YS/040461/00	1	WASHER	CRINKLE M3 BCUCP	4	EA	SEE ITEM 17 FOR ALTN
012	WS/060078/00	1	EJECTORS	WITH PINS 13301(PAIR)	1	EA	
013	AS/001776/00	1	3 WAY SKT	BL/BL/BL 505 PCA 0X	1	EA	
014	087901/00	1	C	LABEL	1	EA	
015					0		A 82008 REF. MOD.RECORD SHEET
016	DS/033528/00	1	R	332R 1% 0.4W 50PPM MR25/VTM	2	EA	R1,R2.
017	QS/022599/00	1	RIVET	1/8" AL/AL 1801-0408 AVD	4	EA	* ALTN TO ITEMS 9,10,11
018	DS/033876/00	1	R	1K 1% 0.4W 50PPM MR25/VTM	4	EA	R3,4,5,6
019	DS/033529/00	1	R	475R 1% 0.4W 50PPM MR25/VTM	2	EA	R7,8
020	DS/034885/00	1	R	562R 1% 0.4W 50PPM MR25/VTM	2	EA	R9,10
021	DS/036111/00	1	RES	PACK 4308R-101-562 BURNS	1	EA	RP1
022	DS/036116/00	1	RES	PACK 764-1-R5K6 BECKMAN	0	EA	* ALTN FOR ITEM 21
023	CS/031998/00	1	CAP	120PF 1% 30V HS SUFLEX	2	EA	C27,29
028	CS/031721/00	1	CAP	0.01MF 10% 100V 8131M100	23	EA	C3 TO 23,25,26
031	CS/031723/00	1	CAP	0.1MFD 10% 100V 8131M100	2	EA	C2,24
033	CS/031745/00	1	CAP	4.7 MF 25V TAG 4.7/25 ITT	1	EA	C1
037	QS/022736/00	1	SWITCH	0N/0FFX8 DIL 24008G WAY	2	EA	8D,12C.
041	091258/00	1	A	LOCKING ROD	2	EA	FOR USE WITH ITEM 37

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
042	BS/003135/00	1	DIÖDE HÖLDER A1136	JERMYN 2	EA	FOR USE WITH ITEM 23
043	BS/005231/00	1	I/C SKT 20PIN 583640-2 AMP	1	EA	FOR MTG.ITEM.91
046	BS/003981/00	1	I/C SN74LS00N TEXAS ONLY	1	EA	12B
049	BS/003983/00	1	I/C SN74LS04N TEXAS ONLY	3	EA	4D,8C,13C.
052	BS/005092/00	1	I/C SN74LS08N OPEN MARKET	3	EA	9A,9B,13B.
055	BS/005030/00	1	I/C SN74LS32N OPEN MARKET	1	EA	7C.
061	BS/005156/00	1	I/C SN74LS42AN OPEN MARKET	1	EA	13A
064	BS/005076/00	1	I/C SN74LS74 OPEN MARKET	4	EA	1C,2D,5D,6D
067	BS/005119/00	1	I/C SN74LS85N OPEN MARKET	2	EA	11D,13D
070	BS/003987/00	1	I/C SN74LS86N TEXAS ONLY	3	EA	3C,7A,7B
073	BS/005121/00	1	I/C SN74LS164N OPEN MARKET	6	EA	1B,2B,2C,3B,4B,4C
076	BS/003541/00	1	I/C SN74LS174N TEXAS ONLY	1	EA	5C,
079	BS/005009/00	1	I/C SN74LS191N TEXAS ONLY	2	EA	9C 10C
080	BS/005120/00	1	I/C SN74LS161N OPEN MARKET	3	EA	5B,6B,6C
082	BS/005001/00	1	I/C SN74LS273N TEXAS ONLY	3	EA	5A,6A,11A,
085	BS/005077/00	1	I/C SN74LS283N OPEN MARKET	2	EA	10A,12A,
088	BS/005227/00	1	I/C SN74S412 TEXAS ONLY	6	EA	1A,1D,2A,3A,3D,4A,
090	BS/005230/00	1	I/C AM8212 AMD ONLY	0	EA	* ALTN FOR ITEM 88
091	088477/00	1	I/C SN74S471N PROGRAMMED	1	EA	8A MAKE FROM BS 5234
094	BS/005233/00	1	I/C P8216 INTEL ONLY	2	EA	9D,10D,
095	BS/006069/00	1	I C GN137 HEW-PACKARD ONLY	1	EA	7D
098	082113/13	1	C BUSBAR,13 LEGS	1	EA	
099	082113/06	1	C BUSBAR,6 LEGS	1	EA	
100	082113/07	1	C BUSBAR,7 LEGS	1	EA	
105	KS/015700/00	1	PIN -75401/002 BERG.	3	EA	FOR LK1

IT COMP. NUMBER S STOCK DESCRIPTION			QTY	UN	NOTES
T01			0		ASSY DRG -B88602
001	088604/00	PCB DRILLED	1	EA	
002	KS/015755/00	TERMINAL PIN 75404-037	16	EA	
003	CS/031721/00	CAP 0.01MF 10% 100V 8131M100	3	EA	C15,22,23
004	BS/005120/00	I/C SN74LS161N OPEN MARKET	3	EA	5B,6B,6C
005	BS/005328/00	I/C IL100 LITRONIX ONLY	1	EA	OPT1
006	DS/033529/00	R 475R 1% 0.4W 50PPM MR25/VTM	1	EA	R7
007	LS/017009/00	KINAR INSUL 1.025MM SIN SPCW	0	M	A/R

PARTS LIST 082041/00				ISSUE 09	C.N.	09634	DATE 18/11/80	C>PCB ASSY, CORRELATOR A/D SE2450	00245000007

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY	UN	NOTES	
038	DS/036401/00	1	RES	10K	1% 1W TR6 ELECTROSIL	1	EA	R23	
039	DS/034095/00	1	R	10K	1% 0.4W 50PPM MR25/VTM	1	EA	R40	
041	DS/034060/00	1	RES	12K1	1% .4W MR25 VTM/471	1	EA	R6	
042	DS/036325/00	1	RES	62K	0.5% 25PPM FC55 AL BRD	1	EA	R41	
043	DS/034075/00	1	RES	18K	1% 1/4W 15PPM FC65	1	EA	R13	
045	DS/034435/00	1	R	990K	0.05% 1/2W 15PPM FC70	1	EA	R21	
046	DS/034899/00	1	RES	20K	.4W MR25 VTM/471	1	EA	R42	
047	DS/036180/00	1	RES	10M	5% 1/2W VR37 MULLARD	1	EA	R34	
049	DS/036303/00	1	RES	PACK	5 X 680 4306R-101-681	4	EA	RP2, RP3, RP5	
050	DS/032058/00	1	RES	470R	5% 2.5W W21 WELWYN	2	EA	R44, 45	
051	FS/010876/00	1	POT:R	500R	10% 1/4W 12T 3262X	1	EA	RV1	
054	FS/010877/00	1	POT:R	10K	10% 1/4W 12T 3262X	2	EA	RV2, 4	
056	FS/010878/00	1	POT:R	50K	10% 1/4W 12T 3262X	1	EA	RV3	
057	FS/010739/00	1	POT	100K	10% 1/4W 3262W-1-104	1	EA	RV5	
058	DS/036308/00	1	RES	PACK	9 X 10K 4310R-101-103	1	EA	RP4	
059	DS/036305/00	1	RES	PACK	5 X 10K 4306R-101-103	1	EA	RP1	
061	CS/032075/00	1	CAP	10PF	2.5% 30V HS SUFLEX	3	EA	C19, 6B (SOT), 11B (SOT)	
064	CS/032725/00	1	CAP	22MF	20% 25V TAG 22/25 ITT	2	EA	C28, C32	
065	CS/030538/00	1	CAP	33PF	5% 30V HS SUFLEX	1	EA	C8	
066	CS/032254/00	1	CAP	22PF	2.5% 30V HS30 SUFLEX	1	EA	C13	
067	CS/031733/00	1	CAP	100PF	2.5% 30V HS SUFLEX	4	EA	C6A (SOT), 12, 15, 21	
068	CS/031739/00	1	CAP	1000 PF	21/2% 30V HS30	1	EA	C22	
069	CS/031735/00	1	CAP	220PF	2.5% 30V HS SUFLEX	1	EA	C20	
070	CS/032223/00	1	CAP	1MF	10% 35V K1/35 U/CARB	2	EA	C80, 81	
071	CS/031721/00	1	CAP	0.01MF	10% 100V 8131M100	50	EA	FOR CIRC. REFS, SEE ITEMS 900 & 901	

IT COMP.	NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
073	CS/031723/00	1 CAP 0.1MFD 10% 100V 8131M100	7	EA	C23, 27, 29, 31, 33, 35, 38
075	CS/031745/00	1 CAP 4.7 MF 25V TAG 4.7/25 ITT	2	EA	C36, 37
076	CS/032840/00	1 CAP 4.7MF 50V 20% TAP 4.7/50	2	EA	C30, 34
077	CS/031731/00	1 CAP 47PF 2.5% 30V HS SUFLEX	1	EA	C11B (S0T)
078	CS/032059/00	1 CAP 68PF 2.5% 30V HS7 SUFLE	1	EA	C11B (S0T)
079	CS/031732/00	1 CAP 82PF 21/2% HS30	1	EA	C11B (S0T)
080	CS/031738/00	1 CAP 680PF 2.5% 30V HS30 SUFLEX	1	EA	C11A (S0T)
081	CS/031814/00	1 CAP 820PF 2.5% 30V HS SUFLEX	1	EA	C11A (S0T)
084	BS/002699/00	1 Z.DIODE 15V 5% 400M/W BZY88C15	2	EA	D7, 8
086	BS/002045/00	1 DIODE 10M/A 100V 1N914 TRANSIT	4	EA	D3, D4, D5, D6
088	BS/002641/00	1 Z.DIODE 20V 5% 400MW BZY88C20	2	EA	D9, 10
091	JS/014080/00	1 LAMP MIN NEON IND 16/30/SB HIV	1	EA	LP1
092	CS/032451/00	1 CAP 15PF 2.5% 63V HS15 SUFLEX	1	EA	C6B (S0T)
093	CS/032340/00	1 CAP 4.7PF 2.5% 30V HS SUFLEX	1	EA	C6B (S0T)
094	CS/032060/00	1 CAP 2.5% 120PF TYPE HS30 SFLEX	1	EA	C6A (S0T)
095	BS/003981/00	1 I/C SN74LS00N TEXAS ONLY	5	EA	7C, 9A, 9E, 13C, 9G
100	BS/003982/00	1 I/C SN74LS02N TEXAS ONLY	2	EA	12A, 12F
103	BS/003983/00	1 I/C SN74LS04N TEXAS ONLY	3	EA	8B, 4F, 13F
105	BS/007406/00	1 I/C SN7406N OPEN MARKET	1	EA	1A
106	BS/005244/00	1 I/C SN74LS21N TEXAS ONLY	1	EA	8C
109	BS/005243/00	1 I/C SN74LS27N TEXAS ONLY	1	EA	11F
112	BS/005008/00	1 I/C SN74LS74N TEXAS ONLY	4	EA	11A, 13A, 11B, 4G.
115	BS/003987/00	1 I/C SN74LS86N TEXAS ONLY	1	EA	12D
118	BS/005240/00	1 I/C SN74LS107N TEXAS ONLY	1	EA	11E
121	BS/005007/00	1 I/C SN74LS157N TEXAS ONLY	1	EA	3F

PARTS LIST 082041/00 ISSUE 09 C.N. 09634 DATE 18/11/80 C>PCB ASSY,CORRELATOR A/D SE2450 00245000007									

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY	UN	NOTES	
124	BS/005354/00	1	I/C	TYPE	SN74LS161N TEXAS ONLY	2	EA	13D,11G	
127	BS/005790/00	1	I.C	SN	74165N TEXAS ONLY	2	EA	11C,11D	
130	BS/005785/00	1	I.C	SN	74H183N TEXAS ONLY	1	EA	12C	
133	BS/005787/00	1	I.C	SN	74LS197N TEXAS ONLY	1	EA	8E	
136	BS/005227/00	1	I/C	SN74S412	TEXAS ONLY	2	EA	3B,5B	
139	BS/006069/00	1	I C	GN137 HEW-PACKARD	ONLY	6	EA	10A,7E,13E,7G,8G,10G	
142	BS/005765/00	1	I.C	HI1-201-5	HARRIS ONLY	2	EA	3E,4E	
150	BS/005767/00	1	I.C	HA2-2645-5	HARRIS ONLY	1	EA	2F	
151	BS/005291/00	1	I/C	SN74LS123N	TEXAS ONLY	1	EA	10E	
152	BS/005979/00	1	I.C	HA2-2535-5	HARRIS ONLY	1	EA	2A	
153	BS/005978/00	1	I.C	HA2-2625-5	HARRIS ONLY	1	EA	2C	
154	BS/005768/00	1	I.C	HA1-2425-5	HARRIS ONLY	1	EA	7D	
157	BS/005770/00	1	I.C	ADC-85C	BURR BROWN	1	EA	10D	
160	BS/005793/00	1	IC	DIG.T0 AN, DAC-05-EX1	PREC.	1	EA	5D	
163	BS/005769/00	1	I.C	1LQ 74	LITRONIX ONLY	4	EA	3C,4C,5C,6B	
164	BS/006109/00	1	I.C.	V0LT.REG	SELECTED A91622	1	EA	REG.1	
165	BS/006108/00	1	I.C.	V0LT.REG	SELECTED A91623	1	EA	REG.2	
166	BS/002263/00	1	MOUNTING	PAD T05-001	JERMYN	2	EA	FOR MTG ITEMS 164,165	
167	BS/002343/00	1	HEAT SINK	5F2 REDPOINT		2	EA	FOR USE WITH ITEMS 164,165	
169	HS/012227/00	1	RELAY	175A-4	ASTRALUX	1	EA	RLA	
170	HS/012226/00	1	RELAY	181A-4	ASTRALUX	1	EA	RLB	
171	BS/003135/00	1	DIODE	HOLDER A1136	JERMYN	22	EA	MTG ITEMS 61,65-69,77-82,84,86,92-94	
172	HS/012233/00	1	REED RELAY	5V 10MA GT66-1A-05-		0	EA	* ALTN TO ITEM 170	
173	KS/015700/00	1	PIN	-75401/002 BERG.		14	EA	TPA-F ,S0T CAPS	
174	WS/028003/00	1	BEADS	CERAMIC N02		10	EA	FOR MTG ITEMS 19,38,50	

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
176	BS/005014/00	1	I/C SKT 16PIN US-2-16-110-N-B	2	EA	FOR MTG. ITEMS 142.
177	BS/005775/00	1	MOUNTING PAD T05-8L-N JERMYN	3	EA	FOR MTG ITEMS 150,152,153
178	BS/005796/00	1	I.C SKT-16 PIN 2302 BURR BROWN	2	EA	FOR MTG ITEM 157
179	BS/005773/00	1	I.C SKT 18 PIN US-2-18-110-N-B	1	EA	FOR MTG ITEM 160
180	ES/008614/00	1	CHØKE R.F 6UH 250V 9W-029817	1	EA	L1
900				0		C9,10,14,16,17,18,24,25,26
901				0		C43 TØ 79,82 TØ 85

PARTS LIST 082051/00 ISSUE 07 C.N. 09625 DATE 29/10/80 C>PCB ASSY,DISPLAY CONTROL 1 SE2450							00245000008	

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY	UN	NOTES
T01						0		NOTE- THIS PL ASSY TO D82051
T02						0		CIRCUIT DIAGRAM E82050
001	PL/087681/00	#	DISPLAY	CONT.1	PCB DRILLED	1	EA	PCB DRILLING
007	087917/00	1	C	LABEL (NUMBER)		1	EA	
008	WS/060079/00	1	PCB	HANDLE	BLACK CH 10036/3	2	EA	
009	YS/040087/00	1	SC	POZ	PAN M3 X 8 MSZP	4	EA	SEE ITEM 17 FOR ALTN
010	YS/040385/00	1	NUT	HEX	FULL M3 MSZP	4	EA	SEE ITEM 17 FOR ALTN
011	YS/040461/00	1	WASHER	CRINKLE	M3 BCUCP	4	EA	SEE ITEM 17 FOR ALTN
012	WS/060078/00	1	EJECTORS	WITH	PINS 13301(PAIR)	1	EA	
013	AS/001776/00	1	3	WAY	SKT BL/BL/BL 505 PCA 0X	4	EA	
014	087904/00	1	C	LABEL (TITLE)		1	EA	
015						0		A 82053 REF MOD. RECORD SHEET
016	BS/003981/00	1	I/C	SN74LS00N	TEXAS ONLY	5	EA	1D,6B,6C,7A,9C
017	QS/022599/00	1	RIVET	1/8"	AL/AL 1801-0408 AVD	4	EA	* ALTN TO ITEMS 9,10,11
019	BS/003982/00	1	I/C	SN74LS02N	TEXAS ONLY	1	EA	9A
022	BS/003983/00	1	I/C	SN74LS04N	TEXAS ONLY	3	EA	2D,5B,7B,
023	BS/005676/00	1	IC	74LS14	TYPE A 97009	1	EA	8E
025	BS/003984/00	1	I/C	SN74LS08N	TEXAS ONLY	4	EA	1A,2C,5C,6D
028	BS/005111/00	1	I/C	SN74LS11N	OPEN MARKET	1	EA	7D
031	BS/003986/00	1	I/C	SN74LS20N	TEXAS ONLY	2	EA	8C,9E
034	BS/005244/00	1	I/C	SN74LS21N	TEXAS ONLY	2	EA	2B,3E
037	BS/005243/00	1	I/C	SN74LS27N	TEXAS ONLY	1	EA	9B
040	BS/005242/00	1	I/C	SN74LS51N	TEXAS ONLY	4	EA	2A,4D,4E,6A
043	BS/005008/00	1	I/C	SN74LS74N	TEXAS ONLY	4	EA	1E,2E,6E,7E
046	BS/005241/00	1	I/C	SN74LS93N	TEXAS ONLY	2	EA	1B,1C

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
049	BS/005240/00 1 I/C SN74LS107N TEXAS ONLY	2	EA	3A,5D
052	BS/004154/00 1 I/C SN74154N OPEN MARKET	1	EA	9D
055	BS/005228/00 1 I/C SN74S157N TEXAS ONLY	4	EA	3C,3D,4C,5E
058	BS/005239/00 1 I/C SN74LS192N TEXAS ONLY	1	EA	7C
061	BS/005003/00 1 I/C SN74LS193N TEXAS ONLY	2	EA	8A,8B
064	BS/005012/00 1 I/C SN74LS283N TEXAS ONLY	2	EA	3B
065	CS/031731/00 1 CAP 47PF 2.5% 30V HS SUFLEX	1	EA	C44
066	CS/031745/00 1 CAP 4.7 MF 25V TAG 4.7/25 ITT	1	EA	C1
068	CS/031723/00 1 CAP 0.1MFD 10% 100V 8131M100	1	EA	C2
069	LS/017009/00 1 KINAR INSUL 1.025MM SIN SPCW	0	M	LK 1-7
070	CS/031721/00 1 CAP 0.01MF 10% 100V 8131M100	41	EA	C3 TO C43
071	DS/033528/00 1 R 332R 1% 0.4W 50PPM MR25/VTM	8	EA	R1-7 INC R12
072	DS/033876/00 1 R 1K 1% 0.4W 50PPM MR25/VTM	4	EA	R8-11 INC
073	DS/034887/00 1 R 1K1 1% 0.4W 50PPM MR25/VTM	1	EA	R13
074	DS/033534/00 1 R 825R 1% 0.4W 50PPM MR25/VTM	1	EA	R14
075	KS/015700/00 1 PIN -75401/002 BERG.	14	EA	
076	BS/003135/00 1 DIODE HOLDER A1136 JERMYN	1	EA	FOR MTG ITEM 65
077	LS/017009/00 1 KINAR INSUL 1.025MM SIN SPCW	0	M	A/R

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
T01				0		NOTE- THIS PL ASSY TO DRG 82056
T02				0		CIRCUIT DIAGRAM E82055
001	PL/086906/00			1		
007	087916/00	C LABEL (NUMBER)		1	EA	
008	WS/060079/00	PCB HANDLE BLACK CH 10036/3		2	EA	
009	YS/040087/00	SC P0Z PAN M3 X 8 MSZP		4	EA	SEE ITEM 17 FOR ALTN
010	YS/040385/00	NUT HEX FULL M3 MSZP		4	EA	SEE ITEM 17 FOR ALTN
011	YS/040461/00	WASHER CRINKLE M3 BCUCP		4	EA	SEE ITEM 17 FOR ALTN
012	WS/060078/00	EJECTORS WITH PINS 13301(PAIR)		1	EA	
013	AS/001776/00	3 WAY SKT BL/BL/BL 505 PCA 0X		2	EA	
014	087903/00	C LABEL (TITLE)		1	EA	
015				0		A82058, MOD. RECORD SHT, REF. ONLY
016	DS/034870/00	RES 75R 1% 0.4W 100PPM MR25		1	EA	R8
017	QS/022599/00	RIVET 1/8" AL/AL 1801-0408 AVD		4	EA	* ALTN TO ITEMS 9,10,11
018	DS/034874/00	RES 121R 1% 0.4W 100PPM MR25		1	EA	R7
020	DS/035673/00	267R 1% 0.4W 50PPM VTM471/MR25		1	EA	R10
022	DS/034885/00	R 562R 1% 0.4W 50PPM MR25/VTM		5	EA	R1,2,4,5,14
023	DS/033534/00	R 825R 1% 0.4W 50PPM MR25/VTM		1	EA	R15
026	DS/033876/00	R 1K 1% 0.4W 50PPM MR25/VTM		5	EA	R3,R9,R11,R12,R13
027	DS/034887/00	R 1K1 1% 0.4W 50PPM MR25/VTM		1	EA	R16
028	DS/036299/00	RES PACK 7 X 2K2 4308R-101-222		1	EA	RP1
030	FS/010468/00	POT 2K ET34P		1	EA	RV1
031	CS/031756/00	CAP 150PF 2.5% 30V HS SUFLEX		1	EA	C2
033	CS/031735/00	CAP 220PF 2.5% 30V HS SUFLEX		1	EA	C1
035	CS/031721/00	CAP 0.01MF 10% 100V 8131M100		43	EA	C10,C12-53 INCL.

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
037	CS/031723/00	CAP 0.1MFD 10% 100V 8131M100		4	EA	C3,C5,C7,C9
039	CS/031745/00	CAP 4.7 MF 25V TAG 4.7/25	ITT	3	EA	C4,C6,C8
042	BS/003177/00	DIODE 10M/A 75V 1N4148 MULLARD		1	EA	D1
044	BS/002694/00	DIODE ZENER 3V6 BZY88 MULLARD		1	EA	D2
046	BS/002838/00	TRANSISTOR MPS3640 MOTOROLA		5	EA	TR1,TR2,TR3 TR4 TR5
050	BS/003981/00	I/C SN74LS00N TEXAS ONLY		3	EA	5A,11A,14C.
053	BS/003982/00	I/C SN74LS02N TEXAS ONLY		5	EA	4A,4C,4D,5B,11B.
056	BS/003983/00	I/C SN74LS04N TEXAS ONLY		3	EA	4B,10B,13D.
061	BS/003984/00	I/C SN74LS08N TEXAS ONLY		3	EA	12A,12B,14D.
064	BS/005589/00	I/C SN74LS10N TEXAS ONLY		1	EA	11D
067	BS/005283/00	I/C SN74LS11N TEXAS ONLY		1	EA	2A
070	BS/003986/00	I/C SN74LS20N TEXAS ONLY		1	EA	3A.
073	BS/005073/00	I/C SN74LS32N TEXAS ONLY		1	EA	5D
076	BS/005352/00	I/C SN74LS42N TEXAS ONLY		1	EA	2D
079	BS/005242/00	I/C SN74LS51N TEXAS ONLY		1	EA	10C
082	BS/005008/00	I/C SN74LS74N TEXAS ONLY		5	EA	6A,12C,12D,13B,13C.
085	BS/005241/00	I/C SN74LS93N TEXAS ONLY		3	EA	8A,14A,14B
088	BS/005783/00	I.C SN 74LS96N TEXAS ONLY		1	EA	13A
091	BS/005240/00	I/C SN74LS107N TEXAS ONLY		4	EA	6B,8B,10A,11C
094	BS/004154/00	I/C SN74154N OPEN MARKET		1	EA	3D.
097	BS/005007/00	I/C SN74LS157N TEXAS ONLY		4	EA	6D,7D,8D,9D,
100	BS/005779/00	I.C SN 74199N OPEN MKT		2	EA	2B,3B
103	BS/005778/00	I.C SN 74S260 OPEN MKT		1	EA	5C
106	BS/005227/00	I/C SN74S412 TEXAS ONLY		1	EA	10D
109	BS/005772/00	I.C MM 6072 MONO-MEMORIES		1	EA	1D

IT COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
112	BS/005771/00	I.C	TMS 3417 TEXAS ONLY	2	EA	6C,9C
115	BS/005777/00	I.C	SN 74100 OPEN MKT	1	EA	1B
117	BS/005014/00	I/C SKT	16PIN US-2-16-110-N-B	2	EA	FOR MTG.ITEM 112
119	BS/005136/00	I/C SKT	24PIN US-2-24-110-N-B	1	EA	FOR MTG.ITEM 109
121	BS/002666/00	MOUNTING PAD	10358 M.ROSS	5	EA	FOR MTG ITEM 46
123	BS/003135/00	DIODE HOLDER	A1136 JERMYN	4	EA	FOR MTG ITEMS[31, 33,42,& 44

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	NOTES
035	CS/031745/00	1	CAP 4.7 MF 25V TAG 4.7/25	ITT 2	C7,9
036	CS/031721/00	1	CAP 0.01MF 10% 100V 8131M100	51	C3,5,6,13 TO 60
040	BS/003177/00	1	DIODE 10M/A 75V 1N4148 MULLARD	1	D1
041	BS/002694/00	1	DIODE ZENER 3V6 BZY88 MULLARD	1	D2
045	BS/002838/00	1	TRANSISTOR MPS3640 MOTOROLA	5	TR1,2,3,4,5
049	BS/005005/00	1	I.C 74LS393N	TEXAS ONLY 3	2A,11A,2D
050	BS/005589/00	1	I/C SN74LS10N	TEXAS ONLY 2	3A,12A
051	BS/005223/00	1	I/C SN74LS01N	TEXAS ONLY 1	5A
052	BS/005008/00	1	I/C SN74LS74N	TEXAS ONLY 4	4A,7A,13A,13B
053	BS/003982/00	1	I/C SN74LS02N	TEXAS ONLY 2	6A,9B
054	BS/005073/00	1	I/C SN74LS32N	TEXAS ONLY 1	9A
055	BS/005240/00	1	I/C SN74LS107N	TEXAS ONLY 4	8A,10A,4B,3C
056	BS/003984/00	1	I/C SN74LS08N	TEXAS ONLY 1	2B
057	BS/003983/00	1	I/C SN74LS04N	TEXAS ONLY 1	3B
058	BS/005242/00	1	I/C SN74LS51N	TEXAS ONLY 2	5B,12B
059	BS/003981/00	1	I/C SN74LS00N	TEXAS ONLY 5	6B,7B,8B,5C,1D
060	BS/005778/00	1	I.C SN 74S260	OPEN MKT 1	10B
061	BS/005283/00	1	I/C SN74LS11N	TEXAS ONLY 2	11B,1C
062	BS/005244/00	1	I/C SN74LS21N	TEXAS ONLY 1	2C
063	BS/003986/00	1	I/C SN74LS20N	TEXAS ONLY 1	4C
064	BS/006064/00	1	I.C 74LS166N	TEXAS ONLY 1	6C
065	BS/005352/00	1	I/C SN74LS42N	TEXAS ONLY 2	7C,8C
066	BS/005228/00	1	I/C SN74S157N	TEXAS ONLY 6	9C,11C,12C,8D,10D,11D
067	BS/006063/00	1	I.C. S67401	MONO MEMORY 2	10C,9D
068	BS/005003/00	1	I/C SN74LS193N	TEXAS ONLY 2	3D,4D

IT COMP.	NUMBER	S STOCK	DESCRIPTION	QTY	NOTES
T01	090221/00	4	D ASSY DRG	0	REF. ONLY
T02	090220/00	4	E CCT DIAG	0	REF. ONLY
001	PL/090226/00	1	PCB DRILLED, PL ONLY	1	
007	087916/00	1	C LABEL (NUMBER)	1	
008	WS/060079/00	1	PCB HANDLE BLACK CH 10036/3	2	
009	YS/040087/00	1	SC P0Z PAN M3 X 8	4	MSZP
010	YS/040385/00	1	NUT HEX FULL M3	4	MSZP
011	YS/040461/00	1	WASHER CRINKLE M3	4	BCUCP
012	WS/060078/00	1	EJECTORS WITH PINS 13301(PAIR)	1	
013	AS/001776/00	1	3 WAY SKT BL/BL/BL 505 PCA 0X	2	
014	088918/00	1	B LABEL-TITLE	1	
015	090223/00	4	A MOD. STATE RECORD SHEET	0	REF. ONLY
017	QS/022599/00	1	RIVET 1/8" AL/AL 1801-0408 AVD	4	* ALTN TO ITEMS 9,10 & 11
018	DS/034870/00	1	RES 75R 1% 0.4W 100PPM MR25	1	R8
019	DS/034874/00	1	RES 121R 1% 0.4W 100PPM MR25	1	R6
020	DS/034885/00	1	R 562R 1% 0.4W 50PPM MR25/VTM	5	R3,4,5,7,9
021	DS/035673/00	1	267R 1% 0.4W 50PPM VTM471/MR25	1	R11
022	DS/033876/00	1	R 1K 1% 0.4W 50PPM MR25/VTM	1	R10
023	DS/034877/00	1	RES 221R 1% 0.4W 100PPM MR25	1	R1
024	DS/033528/00	1	R 332R 1% 0.4W 50PPM MR25/VTM	1	R2
025	DS/034093/00	1	R 5K62 1% 0.4W 50PPM MR25/VTM	2	R13,12
028	FS/010468/00	1	P0T 2K ET34P	1	RV1
032	CS/004597/00	1	CAP 470PF 10% 30V HS7/A SUFLEX	1	C1
033	CS/031142/00	1	CAP 100PF 10% 30V HS SUFLEX	2	C2,61
034	CS/031723/00	1	CAP 0.1MFD 10% 100V 8131M100	3	C4,8,10

IT COMP. NUMBER S STOCK DESCRIPTION			QTY	NOTES
069	BS/005239/00	1 I/C SN74LS192N TEXAS ONLY	1	5D
070	BS/005227/00	1 I/C SN74S412 TEXAS ONLY	1	12D
071	090222/00	1 A I.C. PROGRAMMED (MK2716)	1	6D MAKE FROM BS5800
072	BS/003985/00	1 I/C SN74LS14N TEXAS ONLY	1	13C
110	BS/005014/00	1 I/C SKT 16PIN US-2-16-110-N-B	2	FOR MTG ITEM 67
111	BS/005136/00	1 I/C SKT 24PIN US-2-24-110-N-B	1	FOR MTG ITEM 71
112	BS/002666/00	1 MOUNTING PAD 10358 M.ROSS	5	FOR MTG ITEM 45
113	BS/003135/00	1 DIODE HOLDER A1136 JERMYN	5	FOR MTG ITEMS 32,33,40,41
120	KS/015700/00	1 PIN -75401/002 BERG.	12	FOR LK 1 TO 4& TPA,B,C,D
122	LS/017009/00	1 KINAR INSUL 1.025MM SIN SPCW	0	100MM FOR LK1 TO 4

PARTS LIST 082061/00 ISSUE 12 C.N. 09673 DATE 16/12/80 C>PCB ASSY,MOTHERBOARD SE2450 0024500009						

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY UN NOTES
T01				0		NOTE- THIS PL ASSY TO E82061
T02				0		CIRCUIT DIAGRAM D82060
001	PL/088497/00	#	PCB	DRILLED,PL ONLY	1	EA PCB DRILLED
004	KS/015974/00	1	JACKSCREW	FEMALE M3 86923-1 AM	1	EA
005	KS/015973/00	1	JACKSCREW	MALE M3 86921-1 AMP	1	EA
014	WS/060703/00	1	FOOT	ADHESIVE BACK SJ 5012 3M	9	EA
015				0		A82063,M0D.RECORD SHT,REF.ONLY
016	DS/035737/00	1	1K24 1%	0.4W 50PPM VTM471/MR25	1	EA R1
017	CS/032445/00	1	CAP	2200MF +50-10% 16V EN12-35	1	EA C1
018	DS/035455/00	1	R	CHIP 899-5-R220/R330 BECKMAN	2	EA RP1,2
019	DS/035458/00	1	390R	CHIP 899-1 R390 BECKMAN	1	EA RP4
021	AS/002688/00	1	KEY	POLARIZING PCP 4G E3 B1CC	24	EA FOR USE WITH ITEM 27
022	AS/002641/00	1	PLUG	6 WAY HEAD 65501-106 BERG	6	EA PL24,25,29
023	AS/002643/00	1	PLUG	13 WAY HDR 65501-113 BERG	6	EA PL26,27,28
024	AS/002642/00	1	PLUG	19 WAY HDR 65501-119 BERG	2	EA PL20
025	AS/002571/00	1	CONN	2+29 WAY 2-825456-9 A.M.P	1	EA PL18.
026	AS/002577/00	1	CONN	8 WAY A.2391 09-72-1081	1	EA PL21
027	AS/002762/00	1	SKT	FXD 60 WAY PCCD30#04GE00J0	24	EA SK1A-13A,SK1B-8B,11B-13B
028	BS/006057/00	1	I/C	SKT 14 PIN US-2-14-160-NB	4	EA FOR MTG ITEMS 18 & 19
029	AS/002576/00	1	CONN	4 WAY A-2391 09-72-1041	1	EA PL33
030	KS/015700/00	1	PIN	-75401/002 BERG.	4	EA
031	DS/036345/00	1	RES	PACK 13<2K2 899-1-R-2K2 BK	1	EA RP3
032	LS/017009/00	1	KINAR	INSUL 1.025MM SIN SPCW	0	M 1600MM
033	AS/002763/00	1	CONN	60WAY MHD32DN0909ML/M31	0	EA * ALTN TO ITEM 27,USE WITH ITEM 34
034	AS/002761/00	1	POLARIZING	KEY ML/BK PYE	0	EA * ALTN TO ITEM 27,USE WITH ITEM 33

IT	COMP.	NUMBER	S	STOCK	DESCRIPTION	QTY	UN	NOTES
T01						0		NOTE- THIS PL ASSY TO D81222
T02						0		INSTALLATION DRG E81220
001	PL/082091/00				Keyswitch 2 Board	1		
002	PL/082086/00				Keyboard 1 CTL. LGC.Board	1		
003	PL/082323/00				Keyboard Cableform Assembly	1		
005	PL/086878/00					1		
007	081207/00				C KEYBOARD RUNNER	2	EA	
008	081182/00				C KEYBOARD COVER	1	EA	
009	082321/00				A SPACER, LONG	4	EA	
013	082756/00				B SPINDLE BUSH	2	EA	
016	YS/040087/00				SC PØZ PAN M3 X 8 MSZP	2	EA	
017	YS/040086/00				SC PØZ PAN M3 X 6 MSZP	4	EA	
018	YS/040464/00				WASHER CRINKLE M6 BCUCP	2	EA	
019	YS/040461/00				WASHER CRINKLE M3 BCUCP	8	EA	
020	YS/040388/00				NUT HEX FULL M6 MSZP	2	EA	
021	YS/040600/00				SC CAP SKT M3 6 MS.PK.BK	2	EA	
024	KS/015309/00				SPIRØL PINS 2.0MMX12MM LG MBK	2	EA	
026	WS/028809/00				SPRING 62403	2	EA	
027	AS/002694/00				CLIP PLG & SKT 86694-8 AMP	1	EA	
028	NS/020215/00				CIRCLIP EXT-SER:E:DN1500 019MS`	4	EA	
029	ØS/021312/00				GRØMMET STRIP:SLITRØUND:544	0	FT	60 MM LG
030	SS/024321/00				ADHESIVE TYPE IS496 LØCTITE	0	EA	A/R
031	082757/00				B SPINDLE BUSH	2	EA	
032	082330/00				A SPINDLE BEARING	2	EA	

PARTS LIST 082086/00 ISSUE 11 C.N. 09630 DATE 10/11/80 C>KEYBOARD 1, CONTROL LOGIC PCB SE2450						0024500010

IT COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
T01				0		NOTE-THIS PL ASSY TO D82086
001	PL/087582/00	#	PCB DRILLED, CON. LOGIC, PL ONLY	1	EA	PCB DRILLED
015				0		A 82088 REF MOD. RECORD SHEET.
016	DS/034857/00	1	RES 22.1R 1% 0.4W 100PPM MR25	1	EA	R5
019	DS/033529/00	1	R 475R 1% 0.4W 50PPM MR25/VTM	1	EA	R8
021	DS/033876/00	1	R 1K 1% 0.4W 50PPM MR25/VTM	3	EA	R4, 13, 14
022	DS/033538/00	1	R 2K21 1% 0.4W 50PPM MR25/VTM	3	EA	R1, R2, R3
023	DS/034894/00	1	R 3K32 1% 0.4W 50PPM MR25/VTM	1	EA	R6
024	DS/034897/00	1	R 4K75 1% 0.4W 50PPM MR25/VTM	1	EA	R7
026	DS/034900/00	1	R 27K4 1% 0.4W 50PPM MR25/VTM	1	EA	R16
027	DS/034912/00	1	RES 130K 1% 0.4W 100PPM MR25	1	EA	R17
028	DS/034095/00	1	R 10K 1% 0.4W 50PPM MR25/VTM	2	EA	R15, 18
029	DS/034849/00	1	R 10R0 1% 0.4W 50PPM MR25/VTM	1	EA	R19
030	DS/036111/00	1	RES PACK 4308R-101-562 BOURNS	1	EA	RP1
032	CS/031735/00	1	CAP 220PF 2.5% 30V HS SUFLEX	1	EA	C6
034	CS/030629/00	1	CAP 2200PF 2.5% 30V HS 2200	1	EA	C5
037	CS/031721/00	1	CAP 0.01MF 10% 100V 8131M100	18	EA	C3, 4, 17 TO 30, 32, 34
038	CS/032390/00	1	CAP 0.022MF 10% 100V 8131M ERI	1	EA	C1
040	CS/031539/00	1	CAP 0.1MF 8131M10010030MW5R0	2	EA	C12, C13.
043	CS/031495/00	1	CAP 4.7MFD 10% 35V TAG4.7/35	3	EA	C10, 11, 31
045	CS/031659/00	1	CAP 47MF 20% 16V TAG47/16 ITT	1	EA	C2
046	CS/032915/00	1	CAP 0.22MF -20+80% 50V ITT	1	EA	C33
048	BS/003135/00	1	DIODE HOLDER A1136 JERMYN	2	EA	FOR MTG. ITEMS 32, 34
050	QS/022736/00	1	SWITCH ON/OFFX8 DIL 24008G WAY	2	EA	INTERRUPT REQUEST & ADDRESS SELECT.
051	091258/00	1	A LOCKING ROD	2	EA	FOR USE WITH ITEM 50

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
053	BS/005014/00	1	I/C SKT 16PIN US-2-16-110-N-B	2	EA	FOR MTG ITEM 88
054	BS/005211/00	1	I/C SKT 28PIN US-2-28-110NB	1	EA	FOR MTG ITEM 94
055	BS/005126/00	1	I/C SKT 40WAY US2-40-110-N-B	1	EA	FOR MTG ITEM 97
057	AS/002239/00	1	SOCKET 38WAY. 1-86063-5	1	EA	SK 1
059	KS/015804/00	1	TERMINAL PIN. 75401-008	12	EA	FOR INTER-BOARD CONNECTIONS A-M
061	BS/003981/00	1	I/C SN74LS00N TEXAS ONLY	2	EA	3E,4A
064	BS/005223/00	1	I/C SN74LS01N TEXAS ONLY	1	EA	2E.
067	BS/003982/00	1	I/C SN74LS02N TEXAS ONLY	1	EA	2B
068	BS/007404/00	1	I/C SN7404N OPEN MARKET	1	EA	2C
070	BS/003983/00	1	I/C SN74LS04N TEXAS ONLY	3	EA	1B,3B,4B
076	BS/005011/00	1	I/C SN74LS85N TEXAS ONLY	2	EA	4E,5E.
082	BS/005225/00	1	I/C SN 74145N TEXAS ONLY	1	EA	1A
088	088478/00	1	C SN74S288 PROGRAMMED	1	EA	MAKE FROM BS5513,5A
089	088479/00	1	C SN74S288 PROGRAMMED	1	EA	MAKE FROM BS5513,5A
091	BS/002955/00	1	I/C CA3086 RCA ONLY	1	EA	2A
094	BS/005222/00	1	I/C MM5873 LICON ONLY	1	EA	3C
097	BS/005221/00	1	I/C 8255 INTEL ONLY	1	EA	5C
098	BS/006071/00	1	I.C LM306P TEXAS ONLY	1	EA	1E
099	BS/003192/00	1	TRANSISTOR BC184 TEXAS	1	EA	TR1
101	BS/002968/00	1	MOUNTING PAD T05/18/002 JERMYN	1	EA	FOR MTG ITEM 99

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01		0		NOTE - THIS PL ASSY TO D82091
001	PL/087731/00 # PCB DRILLED,KEYSWITCH,PL ONLY	1	EA	PCB DRILLED
014		0		A82093,MOD.RECORD SHT,REF.ONLY
015	082675/00 1 C KEYBOARD CAP SET	1	EA	
016	081203/00 1 C KEYBOARD CHASSIS	1	EA	
017	082322/00 1 A SPACER,SHORT	4	EA	
019	DS/034877/00 1 RES 221R 1% 0.4W 100PPM MR25	1	EA	R1
021	CS/030629/00 1 CAP 2200PF 2.5% 30V HS 2200	1	EA	C2
022	CS/031721/00 1 CAP 0.01MF 10% 100V 8131M100	2	EA	C1,C3.
024	BS/003177/00 1 DIODE 10M/A 75V 1N4148 MULLARD	7	EA	D1-D7
027	BS/005225/00 1 I/C SN 74145N TEXAS ONLY	1	EA	IC1
029	QS/022665/00 1 KEYSWITCH 54/000/2 LICON	34	EA	
031	AS/002236/00 1 TERMINAL SOCKET 75302-001	12	EA	FOR INTER BOARD CONNECTIONS A-M
034	BS/003135/00 1 DIODE HOLDER A1136 JERMYN	8	EA	FOR MTG ITEMS 21 & 24
036	YS/040089/00 1 SC P0Z PAN M3 X 12 MSZP	4	EA	
037	YS/040461/00 1 WASHER CRINKLE M3 BCUCP	4	EA	

PARTS LIST 081218/00				ISSUE 01	C.N.	DATE 07/06/79	C>KEYSWITCH ASSY SE 2450	3031040000

IT COMP.		NUMBER S	STOCK DESCRIPTION	QTY	UN	NOTES		
T01				0		NOTE-THIS PL ASSY TO DRG D81218		
T02				0		INSTALLATION DRG D82091		
001	081203/00	C	KEYBOARD CHASSIS	1	EA			
003	QS/022665/00		KEYSWITCH 54/000/2	34	EA			
			LICON					
005	082675/00	C	KEYBOARD CAP SET	1	EA			

9.48

IT COMP.	NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01			1		NOTE- THIS PL ASSY TO E81221 CCT DIAG-E82070
T02			0		
001	PL/082071/00	# POWER SUPPLY PCB NO.1 ASSY	1	EA	
002	PL/082076/00	# POWER SUPPLY PCB NO.2 ASSY	1	EA	
003	PL/082081/00	# P.S.MOTHERBOARD ASSY	1	EA	
004	PL/091121/00	# TOROIDAL TRANS.CABLEFORM ASSY	1	EA	
005	PL/086841/00	# BOTTOM BRACKET ASSY	1	EA	
006	PL/086844/00	# TOP BRACKET ASSY	1	EA	
007	PL/086986/00	# END PLATE SCREENED	1	EA	
008	PL/084856/00	# SWITCH COVER SCREENED	1	EA	
009	081217/00	1 E BACK PANEL CASTING	1	EA	
010	PL/091122/00	# P.S.CABLEFORM ASSY NO.1	1	EA	
011	082339/00	1 B CAP CLAMP	1	EA	
012	PL/091135/00	# P.S.CABLEFORM ASSY NO.2	1	EA	
013	086856/00	1 A SPACER,SHORT,HEX	2	EA	
014	086857/00	1 A SPACER, LONG,HEX	2	EA	
015	045303/00	1 C LIGHTNING FLASH	1	EA	
016	086859/00	1 A SPACER,PCB	4	EA	
018	082666/00	1 A POWER INPUT LABEL	1	EA	
019	086845/00	1 C BOTTOM PLATE	1	EA	
020	086846/00	1 C TOP COVER	1	EA	
023	PL/088962/00	# EARTH LINK ASSY	1	EA	
027	WS/060751/00	1 FAN 115V 50/60HZ 11W SU2A1 ROT	1	EA	
028	RS/023049/00	1 FUSE HOLDER L1382 BEL-LEE	1	EA	
030	RS/023148/00	1 W FUSE HOLDER E6011	3	EA	

PARTS LIST 081221/00 ISSUE 10 C.N. 09660 DATE 11/11/80 C>POWER SUPPLY ASSY SE2450									

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES		
031	WS/060696/00	1	MAINS FILTER 250V 6A L2131B/L	1	EA				
033	QS/022673/00	1	SW PUSH BUT DPDT KPA206N WAYCM	1	EA		SW1		
034	QS/022600/00	1	SWITCH.DPDT.MAIN.S-5022-CD04-0	1	EA		SW2		
036	BS/003508/00	1	INSULATING COVER A22-2003-T03	3	EA				
037	BS/003426/00	1	MOUNTING BUSH A22-2001 JERMYN	6	EA				
038	NS/019989/00	1	WASHER 3MM.I/D A26-3023	3	EA				
039	BS/005279/00	1	HEAT SINK MTG KIT A26-2006	1	EA				
040	BS/003381/00	1	HEATSINK DSF1 REDPOINT	1	EA				
043	NS/020232/00	1	STUD AJ4-60/PP1 DZUS	3	EA				
044	OS/020512/00	1	W HALF GROMMET GP4 PLASTIC	3	EA				
045	TS/025240/00	1	O RING BS1806-008 DZVS	3	EA			FOR MTG ITEM 43	
046	CS/032733/00	1	CAP 10,000 MF +50-10% 25V ERIE	2	EA		C25, C29		
048	BS/003584/00	1	TRANSISTOR MJ2501 MOTOROLA	2	EA		TR10, TR12		
049	BS/005761/00	1	TRANSISTOR 2N5038 RCA	1	EA		TR15		
050	BS/005759/00	1	DIODE STUD MTG IN 3890R RCA	1	EA		D29		
052	BS/003756/00	1	DIODE BRIDGE 26MB5 INT.RECT.	3	EA		D22, D25, D27		
054	DS/034585/00	1	1K 2% 1W TR6	1	EA		R66		
057	RS/023304/00	1	FUSE LINK 4A 19195/4A LITTLE	1	EA		FS12		
058	RS/023305/00	1	FUSE LINK 2.5A L2080A/2,5A B&L	1	EA		FS11		
059	RS/023023/00	1	CARTRIDGE FUSE 15A L 1055 BELL	1	EA		FS13		
068	KS/015966/00	1	TERMINAL RING TONGUE BY-18B-5	2	EA				
069	KS/015964/00	1	TERMINAL RING TONGUE BY-14B-3	3	EA				
072	SS/024321/00	1	ADHESIVE TYPE IS496 LOCTITE	0	EA		A/R		
077	KS/015533/00	1	SOLDER TAG 2BA 2188 R.COURTNEY	1	EA				
078	YS/040107/00	1	SC P6Z PAN M5 X 16 MSZP	1	EA				

IT COMP. NUMBER S STØCK DESCRIPTION				QTY	UN	NOTES
081	YS/040895/00	1	SCREW PØZ PAN M4 X 55LG ST Z&P	4	EA	
082	YS/040097/00	1	SC PØZ PAN M4 X 12	MSZP 4	EA	
083	YS/040096/00	1	SC PØZ PAN M4 X 10	MSZP 1	EA	
084	YS/040089/00	1	SC PØZ PAN M3 X 12	MSZP 2	EA	
085	YS/040095/00	1	SC PØZ PAN M4 X 8	MSZP 4	EA	
086	YS/040092/00	1	SC PØZ PAN M3 X 25	MSZP 1	EA	
087	YS/040087/00	1	SC PØZ PAN M3 X 8	MSZP 3	EA	
088	YS/040090/00	1	SC PØZ PAN M3 X 16	MSZP 6	EA	
089	YS/040003/00	1	SC PØZ CSK M3 X 8	MSZP 2	EA	
090	YS/040086/00	1	SC PØZ PAN M3 X 6	MSZP 10	EA	
091	YS/040006/00	1	SC PØZ CSK M3 X 16	MSZP 2	EA	
094	YS/041428/00	1	SC PØZ B CSK SLFTAP 3/16 STLCP	8	EA	
099	YS/040387/00	1	NUT HEX FULL M5	MSZP 2	EA	
100	YS/040386/00	1	NUT HEX FULL M4	MSZP 4	EA	
101	YS/040385/00	1	NUT HEX FULL M3	MSZP 10	EA	
106	YS/040403/00	1	WASHER STD M5 HEAVY	MSZP 1	EA	
107	YS/040402/00	1	WASHER STD M4 HEAVY	MSZP 3	EA	
108	YS/040401/00	1	WASHER STD M3 HEAVY	MSZP 6	EA	
113	YS/040462/00	1	WASHER CRINKLE M4	BCUCP 6	EA	
114	YS/040461/00	1	WASHER CRINKLE M3	BCUCP 22	EA	
118	YS/040435/00	1	WASHER SHK/PRF M5 INT/T	MSCP 5	EA	
119	YS/040434/00	1	WASHER SHK/PRF M4 INT/T	MSCP 8	EA	
120	YS/040433/00	1	WASHER SHK/PRF M3 INT/T	MSCP 6	EA	
121	LS/017036/00	1	W WIRE 24/0.2 61-12 PT6 T2 BK	0	M	50MM
135	YS/040014/00	1	SC PØZ CSK M4 X 16	MSZP 1	EA	

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
136	OS/020613/00	1	SLEEVE 3X20 PINK H/MAN H30	2	M	
138	OS/020993/00	1	SLVNG TH/FIT 6,35 WH SCL RAYCH	1	M	
158	SS/024248/00	1	HEATSINK COMPOUND DP2623	0	EA	A/R

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01		0		NOTE - THIS PL ASSY TO D82071 CIRCUIT DIAGRAM E82070
T02		0		
001	PL/087701/00	1		
008		0		A 82073 REF MOD RECORD SHEET
012	DS/036332/00 RES 1R2 10% 2.5W W21 WELWYN	2	EA	R6,11
013	DS/036333/00 RES 1R2 10% 2.5W 74EV ERG	0	EA	* ALTN TO ITEM 12
014	DS/034760/00 2R7 5% 2.5W W21 WELWYN	2	EA	R2,9
016	DS/034877/00 RES 221R 1% 0.4W 100PPM MR25	2	EA	R1,R15
018	DS/035786/00 R 4K02 1% 0.4W 50PPM MR25/VTM	4	EA	R3,7,10,14
020	DS/035843/00 RES 15K8 1% 0.4W 50PPM VTM471/	2	EA	R4,12
022	DS/034097/00 R 24K3 1% 0.4W 50PPM MR25/VTM	2	EA	R5,13
027	CS/030264/00 CAP 47PF 5% 160V HS SUFLEX	2	EA	C7,C15
029	CS/031596/00 CAP 0.22MFD 10% 100V 344-21224	2	EA	C2,C18
031	CS/032840/00 CAP 4.7MF 50V 20% TAP 4.7/50	4	EA	C5,8,13,16
033	CS/031744/00 CAP 10MF 20% 35V TAG 10/35 ITT	2	EA	C4,C12
035	CS/032859/00 CAP 470MF -10<50% 63V EN12 ITT	4	EA	C3,6,11,14
037	CS/031280/00 CAP 1500MF +50-10% 017-15152	2	EA	C1,C17
042	BS/005701/00 Z.DIODE 6V2 5W IN5341 B MOTRA	2	EA	D2,D16
044	BS/003561/00 LED T1L209 T1 SUPPLY	7	EA	D3,5,7,10,12,14,17
046	BS/005734/00 BRIDGE RECT 1.2A 400V 1KAB40	6	EA	D1,4,6,11,13,15.
052	BS/002795/00 TRANSISTOR 2N4919 MOTOROLA	4	EA	TR1,TR2,TR3,TR4.
055	FS/010755/00 POT 5K 81E/5K ALLEN BRADLEY	4	EA	RV1,RV2,RV3,RV4,
057	BS/005710/00 IC LM340T-50 NATIONAL ONLY	2	EA	REG1,REG3
059	BS/005706/00 IC LM104H NATIONAL ONLY	2	EA	REG 4,6
061	BS/005707/00 IC LM105H NATIONAL ONLY	2	EA	REG 5,7

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
063	RS/023289/00	FUSE LINK 20MM 250MA L1427A		4	EA	FS3,FS4,FS6,FS7
065	RS/023290/00	FUSE LINK 20MM 500MA L1427A		3	EA	FS2,FS5,FS8
067	RS/023133/00	FUSEHOLDER L1426		7	EA	FOR MTG ITEMS 63 & 64
069	BS/003135/00	DIODE HOLDER A1136	JERMYN	2	EA	FOR MTG ITEM 27
071	BS/005356/00	HEATSINK TV4 REDPOINT		2	EA	FOR MTG ITEMS 57
073	BS/005597/00	HEATSINK T0220 TV1500 REDPOINT		4	EA	FOR MTG ITEM 52
075	BS/002343/00	HEAT SINK 5F2 REDPOINT		4	EA	FOR ITEMS 59 & 61
076	BS/003172/00	I/C MOUNTING PAD MON 8L JERMYN		2	EA	FOR MTG. ITEM 61
078	BS/005061/00	TRANSISTOR MTG PAD MON10/LF		2	EA	FOR MTG. ITEM 59
080	AS/002575/00	CONN 6 WAY A2391 09-72-1061 MX		1	EA	PL2
082	AS/002577/00	CONN 8 WAY A.2391 09-72-1081		1	EA	PL1
084	WS/028003/00	BEADS CERAMIC N02		8	EA	FOR MTG. ITEMS 12&14
086	WS/060685/00	"H"COLUMN INJ MOULDING H3	EMA	0	EA	135MM LG FOR LOCATING ITEMS 71 & 73
087	YS/040215/00	SC P0Z PAN M3 10	MSCHP	6	EA	
096	YS/040461/00	WASHER CRINKLE M3	BCUCP	6	EA	
100	YS/040385/00	NUT HEX FULL M3	MSZP	6	EA	
102	OS/020220/00	LACING CORD NYLON BLACK R88W		0	RL	A/R

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01		0		NOTE - THIS PL ASSY TO D82076.
T02		0		CIRCUIT DIAGRAM NO E82070
001	PL/087711/00	1		
008		0		A 82078 REF MOD RECORD SHEET
012	DS/033609/00 RES 0R10 5% 2.5W W21 WELWYN	2	EA	R57,R65
013	DS/036328/00 RES 0R1 15% 2.5W 74EV 2E56-2.5	0	EA	* ALTN TO ITEM 12
014	DS/034639/00 0R30 10% 2.5W W21	1	EA	R35
016	DS/034783/00 0R50 5% 2.5W W21 WELWYN	1	EA	R40
018	DS/034760/00 2R7 5% 2.5W W21 WELWYN	2	EA	R24 R20
020	DS/034849/00 R 10R0 1% 0.4W 50PPM MR25/VTM	2	EA	R33,R16
022	DS/034857/00 RES 22.1R 1% 0.4W 100PPM MR25	1	EA	R54
024	DS/034858/00 RES 24.3R 1% 0.4W 100PPM MR25	1	EA	R32
028	DS/034861/00 RES 33.2R 1% 0.4W 100PPM MR25	1	EA	R39
031	DS/035003/00 5.10HMS 10% W21 WELWYN	1	EA	R50
033	DS/034869/00 RES 68.1R 1% 0.4W 100PPM MR25	2	EA	R17,R51
035	DS/034872/00 R 100R 1% 0.4W 50PPM MR25/VTM	2	EA	R63,R64
037	DS/034877/00 RES 221R 1% 0.4W 100PPM MR25	1	EA	R60
039	DS/034880/00 RES 365R 1% 0.4W 100PPM MR25	2	EA	R38,R61
041	DS/034884/00 R 511R 1% 0.4W 50PPM MR25/VTM	3	EA	R37,R44,R48
043	DS/034430/00 R 909R 1% 0.4W 50PPM MR25/VTM	1	EA	R18
048	DS/034891/00 RES 1K62 1% 0.4W 100PPM MR25	1	EA	R22
050	DS/035786/00 R 4K02 1% 0.4W 50PPM MR25/VTM	2	EA	R21,27
052	DS/033538/00 R 2K21 1% 0.4W 50PPM MR25/VTM	1	EA	R42
054	DS/035773/00 2K94 1% 0.4W 50PPM VTM471/MR25	1	EA	R58
056	DS/033539/00 R 5K11 1% 0.4W 50PPM MR25/VTM	1	EA	R67

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
058 DS/035799/00	5K49 1% 0.4W 50PPM VTM471/MR25	1	EA	R59
061 DS/035803/00	6K04 1% 0.4W 50PPM VTM471/MR25	1	EA	R31
063 DS/034314/00	R 9K09 1% 0.4W 50PPM MR25/VTM	1	EA	R30
065 DS/034095/00	R 10K 1% 0.4W 50PPM MR25/VTM	2	EA	R53,R43
067 DS/034060/00	RES 12K1 1% .4W MR25 VTM/471	1	EA	R36
069 DS/035846/00	16K9 1% 0.4W 50PPM VTM471/MR25	1	EA	R25
071 DS/034219/00	R 18K2 1% 0.4W 50PPM MR25/VTM	2	EA	R34,56
073 DS/035854/00	R 20K5 1% 0.4W 50PPM MR25/VTM	1	EA	R19
076 DS/034900/00	R 27K4 1% 0.4W 50PPM MR25/VTM	1	EA	R26
077 DS/034100/00	R 39K2 1% 0.4W 50PPM MR25/VTM	1	EA	R71
078 DS/033962/00	R 1M 5% 1/4W CR25 MULLARD	4	EA	R28,R29,R41,R47
079 DS/034875/00	RES 130R 1% 0.4W 100PPM MR25	1	EA	R62
080 DS/034871/00	RES 90.9R 1% 0.4W 100PPM MR25	1	EA	R23
081 DS/035873/00	R 32K4 1% 0.4W 50PPM MR25/VTM	1	EA	R45
082 DS/034093/00	R 5K62 1% 0.4W 50PPM MR25/VTM	1	EA	R46
083 DS/034887/00	R 1K1 1% 0.4W 50PPM MR25/VTM	2	EA	R49,R52
087 FS/010592/00	POT 2.2KOHMS CERMET CMP/PC	1	EA	RV7
089 FS/010755/00	POT 5K 81E/5K ALLEN BRADLEY	3	EA	RV5,RV6,RV8
091 CS/032076/00	CAP 68PF 2.5% 63V HS SUFLEX	1	EA	C23
093 CS/031721/00	CAP 0.01MF 10% 100V 8131M100	1	EA	C36
094 CS/032736/00	CAP 0.22 MF 10% 100V 8131-M100	1	EA	C45
095 CS/032060/00	CAP 2.5% 120PF TYPE HS30 SFLEX	1	EA	C34
097 CS/031723/00	CAP 0.1MFD 10% 100V 8131M100	1	EA	C33
099 CS/031042/00	CAP 4.7MF 20% 35V TAG4.7/351TT	2	EA	C37,C40
101 CS/031744/00	CAP 10MF 20% 35V TAG 10/35 ITT	2	EA	C20,C27

IT COMP. NUMBER S STOCK DESCRIPTION						QTY	UN	NOTES
102	CS/032726/00	CAP 10MF 20% 50V TAP 10/50	ITT	2	EA		C21, C24.	
103	CS/032663/00	CAP 22MFD 20% 35V TAP22-35		3	EA		C28, 30, 38	
105	CS/032735/00	CAP 1 MF 10% 100V 344-21105	ML	1	EA		C32	
106	CS/032724/00	CAP 68MF 20% 25V TAA 68M25D		1	EA		C26	
108	CS/031313/00	CAP 330MF +50710% 017-18331		2	EA		C19, C22	
110	CS/031271/00	CAP 2200MF +50710% 017-14222		1	EA		C39	
116	BS/003031/00	Z.DIODE 5.6V 5% 400M/W BZY88		1	EA		D33	
118	BS/003101/00	Z.DIODE 6.2V 5% 400M/W BZY88		3	EA		D28, D30, D34	
120	BS/002293/00	DIODE 1A 100V 1N4002	MOTOROLA	2	EA		D23, D35	
124	BS/003561/00	LED T1L209 T1 SUPPLY		5	EA		D19, D21, D24, D26 D32.	
126	BS/005734/00	BRIDGE RECT 1.2A 400V 1KAB40		2	EA		D18, D20.	
130	BS/005213/00	TRANSISTOR 2N2222	TEXAS	1	EA		TR20	
132	BS/003194/00	TRANSISTOR 2N2905A	TEXAS	4	EA		TR6, TR11, TR17 TR18	
134	BS/002795/00	TRANSISTOR 2N4919	MOTOROLA	2	EA		TR5, TR7	
136	BS/003192/00	TRANSISTOR BC184	TEXAS	1	EA		TR8	
138	BS/005740/00	TRANS FET PREFORM T0106	J112	2	EA		TR13, 19	
140	BS/005982/00	F.E.T J176	SILICONIX	2	EA		TR9, 14	
142	BS/005958/00	TRANSISTOR BD787	MOTOROLA	1	EA		TR16	
144	BS/005708/00	IC LM304H	NATIONAL ONLY	1	EA		REG 10	
145	BS/005706/00	IC LM104H	NATIONAL ONLY	1	EA		REG 8	
146	BS/005709/00	IC LM305H	NATIONAL ONLY	2	EA		REG 12, REG11	
147	BS/005707/00	IC LM105H	NATIONAL ONLY	1	EA		REG 9	
148	BS/003515/00	SCR S2800D	RCA	1	EA		CSR1	
151	BS/005704/00	IC 4N27	MOTOROLA ONLY	1	EA		OPT 1	
153	ES/008607/00	CHOKE 10A 1H10-50-10A	DALE	1	EA		L1	

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
155 BS/005705/00	HEATSINK TV21 REDPOINT	2	EA	FOR MTG. ITEM 134
157 BS/005356/00	HEATSINK TV4 REDPOINT	1	EA	FOR MTG ITEM 142
159 BS/003135/00	DIODE HOLDER A1136 JERMYN	8	EA	FOR MTG ITEMS 91, 95, 116, 118, 120
161 WS/028003/00	BEADS CERAMIC NO2	8	EA	FOR MTG ITEM 12
163 RS/023290/00	FUSE LINK 20MM 500MA L1427A	2	EA	FS9, 10
165 RS/023133/00	FUSEHOLDER L1426	2	EA	FOR MTG ITEM 163
166 BS/003172/00	I/C MOUNTING PAD MON 8L JERMYN	3	EA	FOR MTG ITEMS 146 & 147
168 BS/005061/00	TRANSISTOR MTG PAD MON10/LF	2	EA	FOR MTG ITEMS 144 & 145
170 BS/002343/00	HEAT SINK 5F2 REDPOINT	5	EA	FOR ITEMS 144 & 146
172 BS/003116/00	MOUNTING PAD EPX-005 JERMYN	3	EA	FOR MTG ITEMS 136, 138
173 BS/002747/00	TRANSISTOR PAD T05-001	4	EA	FOR MTG ITEM 132
174 BS/002968/00	MOUNTING PAD T05/18/002 JERMYN	1	EA	FOR MTG ITEM 130
175 BS/002420/00	MOUNTING PAD 10171 M.ROSS	2	EA	FOR MTG ITEM 140
176 AS/002576/00	CONN 4 WAY A-2391 09-72-1041	1	EA	PL3
178 AS/002575/00	CONN 6 WAY A2391 09-72-1061 MX	1	EA	PL5
180 AS/002577/00	CONN 8 WAY A.2391 09-72-1081	1	EA	PL4
181 YS/040597/00	SC SLT CH M3 8 ST.S	2	EA	
182 YS/040295/00	SCREW SLT CH M3X10 ST/STL	3	EA	
184 YS/040461/00	WASHER CRINKLE M3	5	EA	
186 YS/040385/00	NUT HEX FULL M3	5	EA	
188 OS/020220/00	LACING CORD NYLON BLACK R88W	0	RL	A/R
190 LS/016017/00	WIRE.5KG RL 22SWG	0	KG	A/R
192 OS/020490/00	SLEEVING TWT22	0	M	A/R

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01		0		NOTE - THIS PL ASSY TO D82081
T02		0		CIRCUIT DIAGRAM E 82070
001	PL/087721/00	1		PCB DRILLED
008		0		REF A82083 MOD RECORD SHEET
009	DS/034060/00 RES 12K1 1% .4W MR25 VTM/471	1	EA	R68
010	DS/035846/00 16K9 1% 0.4W 50PPM VTM471/MR25	1	EA	R69
011	DS/034492/00 R 56K 2% 0.4W 100PPM MR25 MUL	1	EA	R70
012	DS/034877/00 RES 221R 1% 0.4W 100PPM MR25	1	EA	R8
013	CS/031739/00 CAP 1000 PF 21/2% 30V HS30	1	EA	C35
014	CS/032723/00 CAP 2200PF 1% 454-273-2200 ITT	1	EA	C42
015		0		A82023 REF MOD RECORD SHEET
016	CS/032727/00 CAP 0.22MF 10% 100V "WEECON"	1	EA	C10
017	CS/032729/00 CAP 22000MF 25V 2222-106-36223	1	EA	C31
018	CS/031280/00 CAP 1500MF +50-10% 017-15152	1	EA	C9
019	CS/032725/00 CAP 22MF 20% 25V TAG 22/25 ITT	1	EA	C44
021	BS/005701/00 Z.DIODE 6V2 5W 1N5341 B MOTRA	1	EA	D9
023	BS/005734/00 BRIDGE RECT 1.2A 400V 1KAB40	1	EA	D8
025	BS/005710/00 IC LM340T-50 NATIONAL ONLY	1	EA	REG 2
026	BS/003441/00 I/C TIMER NE555V SIGNETS ONLY	1	EA	IC1
027	BS/005356/00 HEATSINK TV4 REDPOINT	1	EA	FOR MTG ITEM 25
029	ES/008607/00 CHOKE 10A 1H10-50-10A DALE	1	EA	L2
031	AS/002572/00 CONN 58 WAY 2-87215-9 A.M.P	1	EA	PL8
032	AS/002580/00 CONN 2X18 WAY PCCD-18K-17GE00	2	EA	SKT6,SKT7.
034	NS/019719/00 CAP CLIP DT2254 MULLARD	1	EA	FOR MTG C31.
035	CS/020220/00 LACING CORD NYLON BLACK R88W	0	RL	

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
038	YS/040295/00	SCREW	SLT CH M3X10 ST/STL	1	EA	
039	YS/040097/00	SC P0Z	PAN M4 X 12	MSZP 2	EA	
040	YS/040098/00	SC P0Z	PAN M4 X 16	MSZP 1	EA	
041	YS/040461/00	WASHER	CRINKLE M3	BCUCP 1	EA	
042	YS/040462/00	WASHER	CRINKLE M4	BCUCP 3	EA	
043	YS/040402/00	WASHER	STD M4 HEAVY	MSZP 6	EA	
044	YS/040385/00	NUT	HEX FULL M3	MSZP 1	EA	
045	YS/040386/00	NUT	HEX FULL M4	MSZP 3	EA	

IT COMP.	NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01			0		ASSY DRG C86872
T02			0		CIRC DIAG D86901
001	088675/00	1 A MONITOR MODULE KIT (BRIMAR)	1	EA	
002	DS/036335/00	1 RES 390R 5% 1.6W PR37-390R MUL	1	EA	R3
003	DS/034010/00	1 R 150R 5% 1/4W CR25 MULLARD	1	EA	R1
004	DS/036406/00	1 RES 10K 10% 1/2W EB A BRADLEY	1	EA	R4
005	DS/036408/00	1 RES 22K 10% 1/2W EB A BRADLEY	2	EA	R5 R6
006	DS/036404/00	1 RES 1K5 10% 1/2W EB A BRADLEY	1	EA	R7
007	DS/034004/00	1 R 47R 5% 1/4W CR25 MULLARD	1	EA	R8
008	DS/033939/00	1 R 33R 5% 1/4W CR25 MULLARD	1	EA	R9
009	DS/034051/00	1 R 390K 5% 1/4W CR25 MULLARD	1	EA	R10
010	DS/033964/00	1 R 1M8 10% 1/4W CR25 MULLARD	1	EA	R11
014	FS/010880/00	1 PGT 4K7 20% 0.15W VN15/4K7 A.B	1	EA	RV5
015	FS/010881/00	1 PGT 2M2 30% 0.15W VN15/2M2 A.B	1	EA	RV7
017	CS/032863/00	1 CAP 1000MF -10<50% 16V EN12-35	1	EA	C1
018	CS/032862/00	1 CAP 2200MF -10<50% 16V EN12-35	1	EA	C2
019	CS/032866/00	1 CAP 1MF -10<50% 500V EN12-12	1	EA	C3
020	CS/032865/00	1 CAP 0.012MF 5% 250V SIEMENS	1	EA	C4
021	CS/032860/00	1 CAP 1MF -10<50% 100V EN12-35	1	EA	C5
022	CS/032914/00	1 CAP 220MF -10<50% 100V EN12/35	1	EA	C6
023	CS/032861/00	1 CAP 220MF -10<50% 25V EN12-12	1	EA	C7
024	CS/032864/00	1 CAP 0.022MF 20% 400V C280CF/	1	EA	C8
025	CS/031738/00	1 CAP 680PF 2.5% 30V HS30 SUFLEX	1	EA	C10
029	BS/005334/00	1 DIODE BA159 I.T.T	1	EA	D1
030	BS/005335/00	1 DIODE MR854 MOTOROLA	1	EA	D2

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
031	BS/005957/00	1	DIODE BY184 MULLARD	1	EA	D3
032	BS/005336/00	1	DIODE BY206 MULLARD	1	EA	D4
037	KS/015700/00	1	PIN -75401/002 BERG.	1	EA	TPX
038	LS/017537/00	1	TY-RAP. TY-23M. T.BETTS	8	M	
039	KS/015082/00	1	COMP TERMINAL 8C126 RING 4BA	1	EA	
040	045303/00	1	C LIGHTNING FLASH	1	EA	
043	AS/002706/00	1	PLUG 6 PIN A1840-09-18-5061 MX	1	EA	P2
048	AS/002626/00	1	HOUSING 12 WAY 09-50-3121 MOLX	1	EA	SK30
049	AS/002579/00	1	TERMINAL CRIMP 08-56-0106 MOL	12	EA	FOR ITEM 38
052	LS/016891/00	1	W WIRE 16/0.2 61-12 PT6 T2 SL	0	M	0.43M
053	LS/016883/00	1	WIRE 16/0.2 TYPE 2 PVC BLACK	0	M	0.77M
054	LS/016885/00	1	WIRE 16/0.2 61-12-PT6-T2 RED	0	M	0.47M
055	LS/016888/00	1	W WIRE 16/0.2 61-12 PT6 T2 GN	0	M	0.30M
056	LS/016887/00	1	W WIRE 16/0.2 61-12 PT6 T2 YL	0	M	0.60M
057	LS/016890/00	1	WIRE 16/0.2 TYPE 2 VIOLT	0	M	0.60M
058	LS/016889/00	1	W WIRE 16/0.2 PVC TYPE 2 BLUE	0	M	0.58M
059	LS/016886/00	1	WIRE 16/0.2 TYPE 2 PVC ORANGE	0	M	0.30M
060	LS/017576/00	1	WIRE RED/GRAN. 16/02 PVC TYPE	0	M	0.41M
061	LS/016895/00	1	WIRE 16/0.2 TYPE 2 RD/BLK	0	M	0.41M
062	LS/016897/00	1	W WIRE 16/0.2 TYPE 2 RD/BLU	0	M	0.43M
063	LS/016896/00	1	W WIRE 16/0.2 TYPE 2 RD/BRN	0	M	0.51M
064	LS/016916/00	1	WIRE 16/0.2 TYPE 2 WHT/ORG	0	M	0.81M
065	LS/016918/00	1	WIRE 16/0.2 TYPE 2 WHT/BLU	0	M	0.51M
066	LS/017579/00	1	WIRE BLUE/GRAN.16/02 PVC TYPE	0	M	0.38M
067	LS/017578/00	1	WIRE BLUE/BRN.16/02 PVC TYPE 2	0	M	0.38M

IT COMP. NUMBER S STOCK DESCRIPTION					QTY	UN	NOTES
068	LS/017580/00	1	WIRE BLK./GRAN. 16/02	PVC TYPE	0	M	0.38M
072	LS/016017/00	1	WIRE.5KG RL 22SWG		0	KG	0.3M
074	LS/017676/00	1	COAX CABLE 75 OHM RF T3188BICC		0	M	0.6M
076	OS/021153/00	1	SLEEVEING RILFILEC GY 6/10	ALCR	0	FT	0.24M
078	SS/024607/00	1	LAQUER AEROSOL CLEAR CPL-397		0	EA	A/R
080	DS/036407/00	1	RES 10K 10% 1/2W	00026/012	0	EA	* ALTN TO ITEM 4 (R4)
081	DS/036409/00	1	RES 22K 10% 1/2W	00026/012	0	EA	* ALTN TO ITEM 5 (R5)
082	DS/036405/00	1	RES 1K5 10% 1/2W	00026/012	0	EA	* ALTN TO ITEM 6 (R6)

IT COMP.	NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01			0		THIS PL ASSY TO B86900
001	PL/086898/00	# C.R.T.P&T PCB DRILLED,PL ONLY	1	EA	
003	FS/010856/00	1 P&T:R 470R 150MW VC15 470R	1	EA	RV2
004	FS/010857/00	1 P&T:R 470R 150MW PT15 WH(5)	0	EA	* ALTN ITEM 3
005	FS/010858/00	1 P&T:R 100K 150MW VC15 100K	1	EA	RV3
006	FS/010859/00	1 P&T:R 100K 150MW PT15 WH(5)	0	EA	* ALTN ITEM 5
007	FS/010860/00	1 P&T:R 1M 150MW VC15 1M	1	EA	RV4
008	FS/010861/00	1 P&T:R 1M 150MW PT15 WH(5)1M	0	EA	* ALTN ITEM 7
009	AS/002773/00	1 CONN 12 WAY 09-72-1121 MOLEX	1	EA	PL30
010	AS/002575/00	1 CONN 6 WAY A2391 09-72-1061 MX	1	EA	PL31

IT COMP. NUMBER S STOCK DESCRIPTION			QTY	UN	NOTES
T01			0		NOTE-PL ASSY TO B86958
001	LS/017242/00	TIN COPPER BRAID6.5MM 334T	0	M	300MM
005	KS/015728/00	SOLDER TAG 2BA G721 TUCKER	2	EA	
009	WS/028145/00	SOLDER 22SWG	0	KG	A/R

IT COMP. NUMBER S STOCK DESCRIPTION QTY UN NOTES

T01			0		ASSY DRG-B88622
001	CS/032733/00	CAP 10,000 MF +50-10% 25V ERIE	1	EA	C2
002	AS/002309/00	CONN.HOUSING 4WAY 09-50-3041	1	EA	SK33
003	BS/005762/00	L.E.D YEL & MTG GRÖM. MV 15354	1	EA	LED
004	AS/002509/00	CONNECTÖR HOUSING 6 WAY MÖLEX	1	EA	SKT 2
005	KS/015987/00	TERMINAL LOÖSE 1381-02-09-1119	5	EA	
006	KS/015986/00	TERMINAL LOÖSE 1380-02-09-2118	1	EA	
007	BS/002427/00	DIÖDE 1A 50V IN4001 MÖTÖRÖLA	1	EA	D6
009	ÖS/020979/00	W SLEEVE 1.5MMX12MMLG M12 BK	2	EA	FÖR D6
010	ÖS/020462/00	SLEEVE, 2MM X 1/2	2	EA	FÖR LED
011	ÖS/020409/00	SLEEVE H50 X1/2 PINK	2	EA	FÖR C2
012	LS/016966/00	TY RAP TY3 THOMAS	24	EA	
013	LS/016886/00	WIRE 16/0.2 TYPE 2 PVC ÖRANGE	1	M	WIRE NÖ.1 400 MM
014	LS/016892/00	W WIRE 16/0.2 61-12 PT6 T2 WH	1	M	WIRE NÖ.2 400 MM
015	LS/016885/00	WIRE 16/0.2 61-12-PT6-T2 RED	1	M	WIRE NÖ.3,4 690 MM
016	LS/016883/00	WIRE 16/0.2 TYPE 2 PVC BLACK	1	M	WIRE NÖ.5,6 690 MM
017	NS/019063/00	CLIP CAPACITÖR TYPE V3/32104/6	1	EA	FÖR MTG ITEM 1
018	YS/040295/00	SCREW SLT CH M3X10 ST/STL	3	EA	
019	YS/040385/00	NUT HEX FULL M3 MSZP	3	EA	
020	YS/040401/00	WASHER STD M3 HEAVY MSZP	3	EA	
021	YS/040461/00	WASHER CRINKLE M3 BCUCP	3	EA	
022	AS/002579/00	TERMINAL CRIMP 08-56-0106 MÖL	4	EA	FÖR SK33

PARTS LIST 082709/00 ISSUE 05 C.N. 09358 DATE 15/02/80 C>CONTROL PANEL ASSY SE2450							3031040001

IT	COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
T01					0		NOTE-THIS PL ASSY TO C82709
001	PL/086768/00				1		
002	QS/022359/00			SWITCH SPOT CTS3/BP/1	1	EA	SW1
003	QS/022702/00			SW DPDT BIASED ON 2A 250V CTM6	2	EA	SW2,SW3
004	MS/018118/00			KNØB CAP PALE BLUE 1450-14/PB	3	EA	
005	MS/018099/00			KNØB BLACK 71-21-1/4	3	EA	
006	FS/010848/00			PØTR 100R LIN 500-100R ERIE	1	EA	RV1
007	FS/010850/00			PØTR 100K LIN 500-100K ERIE	1	EA	RV6
008	FS/010849/00			PØTR 50K LIN 500-50K ERIE	1	EA	RV7
012	AS/002578/00			CØNN 8 WAY 2139 09-50-3081 MØL	1	EA	SKT 21
013	AS/002307/00			CØNN HOUSING 6WAY 09-50-3061	1	EA	SKT 31
014	AS/002579/00			TERMINAL CRIMP 08-56-0106 MØL	14	EA	
015	LS/017537/00			TY-RAP. TY-23M. T.BETTS	9	EA	
018	LS/016883/00			WIRE 16/0.2 TYPE 2 PVC BLACK	0	M	300 MM
019	LS/016895/00			WIRE 16/0.2 TYPE 2 RD/BLK	0	M	250 MM
020	LS/016896/00			W WIRE 16/0.2 TYPE 2 RD/BRN	0	M	300 MM
021	LS/016897/00			W WIRE 16/0.2 TYPE 2 RD/BLU	0	M	250 MM
022	LS/016913/00			W WIRE 16/0.2 61-12 PT6 T2W/BK	0	M	200 MM
023	LS/016915/00			W WIRE 16/0.2 61-12 PT6 T2 W/R	0	M	200 MM
024	LS/016916/00			WIRE 16/0.2 TYPE 2 WHT/ØRG	0	M	300 MM
025	LS/016918/00			WIRE 16/0.2 TYPE 2 WHT/BLU	0	M	300 MM
026	LS/016919/00			WIRE 16/0.2 TYPE 2 WHT/GRY	0	M	200 MM
027	LS/017380/00			PVC 16/0.2 V/W DEF61-12PT6 T2	0	M	250 MM
028	LS/017576/00			WIRE RED/ØRAN. 16/02 PVC TYPE	0	M	250 MM
029	LS/017578/00			WIRE BLUE/BRN.16/02 PVC TYPE 2	0	M	250 MM

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IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
030	LS/017579/00 WIRE BLUE/GRAN. 16/02 PVC TYPE	0	M	250 MM
031	LS/017580/00 WIRE BLK./GRAN. 16/02 PVC TYPE	0	M	250 MM
032	LS/017610/00 WIRE PVC 16/0.2 V10/RED BICC	0	M	250 MM
040	WS/028145/00 SOLDER 22SWG	0	KG	A/R

IT COMP. NUMBER S STOCK DESCRIPTION	QTY	UN	NOTES
T01	0		NOTE- THIS PL ASSY TO DRG C81224
001 PL/082772/00 # BACK PANEL SCREENED	1	EA	
002 PL/082318/00 # RETAINING PLATE	1	EA	
003 PL/086882/00 # CABLEFORM ASSY	1	EA	
004 PL/086883/00 # CABLEFORM ASSY	1	EA	
005 PL/086884/00 # CABLEFORM ASSY	1	EA	
006 PL/086885/00 # EXT.SYNC.CABLEFORM 1 ASSY	1	EA	EXTERNAL SYNC.CABLEFORM 1
007 PL/086949/00 # INPUT PANEL ASSY	1	EA	
008 082786/00 1 B BLANKING PLATE	1	EA	
011 AS/002625/00 1 CONN MINI LATCH 65043-031 BERG	2	EA	SK24, 29
012 AS/002627/00 1 SKT FXD 4 WAY D104.A0.37 SELEC	1	EA	SK35
013 AS/002644/00 1 SKT FIXED 3 WAY D104A040 SELEC	2	EA	SKT 36, SKT 37
014 AS/002719/00 1 SKT BULKHEAD 75R GE37508X GNPR	1	EA	SKT 43
016 AS/002598/00 1 BASE RETAINER ASSY R43-00022-	3	EA	
017 AS/002251/00 1 MINI P.V. CONTACTS 47565	18	EA	
018 KS/015407/00 1 TERMINAL 6BA 475 H.T.D.	1	EA	ET1
019 WS/060682/00 1 LABEL SELF ADHESIVE Y75E BRADY	1	EA	
020 LS/017121/00 1 PVC WIRE 7/0.2 TYPE 2 BLACK	0	M	60MM
021 LS/017673/00 1 CAB 2 CORE SCRNL 12/0.2 EHE 2P	0	M	3M
022 LS/017676/00 1 COAX CABLE 75 OHM RF T3188BICC	0	M	250MM
023 LS/017537/00 1 TY-RAP. TY-23M. T.BETTS	18	M	
024 LS/017392/00 1 WIRE PVC 32/0,2 GN/Y TYPE 3	0	M	200 MM
025 YS/040214/00 1 SC PÖZ PAN M3 8 MSCHP	6	EA	
026 YS/040224/00 1 SCREW PÖZ PAN M4X12 MS CH PLT	2	EA	
027 YS/040385/00 1 NUT HEX FULL M3	6	EA	

IT COMP. NUMBER S	STOCK DESCRIPTION	QTY	UN	NOTES
028	YS/040465/00 1 WASHER CRINKLE M3	6	EA	
029	YS/040412/00 1 WASHER STD M4 HEAVY	2	EA	
030	AS/002717/00 1 CONN 'D' SCREW LOCK KIT 552633	1	EA	(KIT OF 2)
031	YS/040387/00 1 NUT HEX FULL M5	2	EA	
032	YS/040403/00 1 WASHER STD M5 HEAVY	2	EA	
033	YS/040435/00 1 WASHER SHK/PRF M5 INT/T	2	EA	

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
T01				0		THIS PL ASSY TO B86883
001 AS/002636/00	CONN MINI LATCH 26 WAY	BERG	1	EA		SKT 26
002 AS/001650/00	SOCKET 25 WAY DB25S CANNON		1	EA		SKT 38
003 AS/002251/00	MINI P.V. CONTACTS 47565		25	EA		
004 SS/024477/00	PAINT AIR DRYING WH 22 HUMBRÖL		0	LT		A/R
005 LS/017071/00	TY-RAP TYPE TY-51M		2	EA		210 MM
006 LS/016504/00	WIRE 7/0.2 6-12-PT6-T1 BLACK		0	M		210 MM
007 LS/016549/00	WIRE 7/0.2 6-12-PT6-T1 BROWN		0	M		210 MM
008 LS/016548/00	WIRE 7/0.2 6-12-PT6-T1 RED		0	M		210 MM
009 LS/016546/00	WIRE 7/0.2 6-12-PT6-T1 ORANGE		0	M		210 MM
010 LS/016506/00	WIRE 7/0.2 6-12-PT6-T1 GREEN		0	M		210 MM
011 LS/016505/00	PVC WIRE 7/0.2 61-12-PT6-T1 BU		0	M		210 MM
012 LS/016545/00	PVC WIRE 7/0.2 61-12-PT6-T1 SL		0	M		210 MM
013 LS/016560/00	PVC 7/0.2 YELLOW TYPE 1.		0	M		210 MM
014 LS/016561/00	WIRE 7/0.2 6-12-PT6-T1 WHITE		0	M		210 MM
015 LS/016871/00	WIRE 7X0.2 PVC TYPE 1 GREY/BRN		0	M		210 MM
016 LS/016873/00	WIRE 7X0.2 PVC TYPE 1 GRY/ÖRGE		0	M		210 MM
017 LS/016874/00	WIRE 7X0.2 PVC TYPE 1 GREY/GRN		0	M		210 MM
018 LS/016875/00	WIRE 7X0.2 PVC TYPE 1 GREY/BL		0	M		210 MM
019 LS/016877/00	WIRE 7X0.2 PVC TYPE 1 WHT/BRN		0	M		210 MM
020 LS/016878/00	WIRE 7X0.2 PVC TYPE 1 WHT/RED		0	M		210 MM
021 LS/016879/00	WIRE 7X0.2 PVC TYPE 1 WHT/ÖRE		0	M		210 MM
022 LS/016880/00	WIRE 7X0.2 PVC TYPE 1 WHT/GRN		0	M		210 MM
023 LS/016881/00	WIRE 7X0.2 PVC TYPE 1 WHE/BLUE		0	M		210 MM
024 LS/016827/00	WIRE 7/0.2 61-12-PT6-T1 WH/SL		0	M		210 MM

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
025	LS/016860/00 WIRE 7X0.2 PVC TYPE 1 RED/BLUE	0	M	210 MM
026	LS/016819/00 PVC WIRE RED/BROWN SIZE 7/02	0	M	210 MM
027	LS/017275/00 PVC WIRE INS 7/0.2 BLK/BROWN	0	M	210 MM
028	LS/016825/00 BLACK ORANGE 7/0.2	0	M	210 MM
029	LS/017148/00 PVC 7/0.2 VIØ/YELL 61-12PT T1	0	M	210 MM
030	LS/016820/00 WIRE PVC 7/0.2 RED/ORANGE	0	M	210 MM

IT COMP.	NUMBER S	STOCK DESCRIPTION	QTY	UN	NOTES
T01			0		THIS PL ASSY TO B86844
001	AS/002636/00	CONN MINI LATCH 26 WAY	BERG 1	EA	SKT 28
002	AS/001650/00	SOCKET 25 WAY DB25S CANNON	1	EA	SKT 41
003	AS/002251/00	MINI P.V. CONTACTS 47565	25	EA	
004	SS/024477/00	PAINT AIR DRYING WH 22 HUMBRÖL	0	LT	A/R
005	LS/017071/00	TY-RAP TYPE TY-51M	2	EA	
006	LS/016504/00	WIRE 7/0.2 6-12-PT6-T1 BLACK	0	M	140MM
007	LS/016549/00	WIRE 7/0.2 6-12-PT6-T1 BROWN	0	M	140MM
008	LS/016548/00	WIRE 7/0.2 6-12-PT6-T1 RED	0	M	140MM
009	LS/016546/00	WIRE 7/0.2 6-12-PT6-T1 ORANGE	0	M	140MM
010	LS/016506/00	WIRE 7/0.2 6-12-PT6-T1 GREEN	0	M	140MM
011	LS/016505/00	PVC WIRE 7/0.2 61-12-PT6-T1 BU	0	M	140MM
012	LS/016545/00	PVC WIRE 7/0.2 61-12-PT6-T1 SL	0	M	140MM
013	LS/016560/00	PVC 7/0.2 YELLOW TYPE 1.	0	M	140MM
014	LS/016561/00	WIRE 7/0.2 6-12-PT6-T1 WHITE	0	M	140MM
015	LS/016871/00	WIRE 7X0.2 PVC TYPE 1 GREY/BRN	0	M	140MM
016	LS/016873/00	WIRE 7X0.2 PVC TYPE 1 GRY/ØRGE	0	M	140MM
017	LS/016874/00	WIRE 7X0.2 PVC TYPE 1 GREY/GRN	0	M	140MM
018	LS/016875/00	WIRE 7X0.2 PVC TYPE 1 GREY/BL	0	M	140 MM
019	LS/016877/00	WIRE 7X0.2 PVC TYPE 1 WHT/BRN	0	M	140 MM
020	LS/016878/00	WIRE 7X0.2 PVC TYPE 1 WHT/RED	0	M	140 MM
021	LS/016879/00	WIRE 7X0.2 PVC TYPE 1 WHT/ØRE	0	M	140 MM
022	LS/016880/00	WIRE 7X0.2 PVC TYPE 1 WHT/GRN	0	M	140 MM
023	LS/016881/00	WIRE 7X0.2 PVC TYPE 1 WHE/BLUE	0	M	140 MM
024	LS/016827/00	WIRE 7/0.2 61-12-PT6-T1 WH/SL	0	M	140 MM

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
025	LS/016860/00 WIRE 7X0.2 PVC TYPE 1 RED/BLUE	0	M	140 MM
026	LS/016819/00 PVC WIRE RED/BROWN SIZE 7/02	0	M	140 MM
027	LS/017275/00 PVC WIRE INS 7/0.2 BLK/BROWN	0	M	140 MM
028	LS/016825/00 BLACK ORANGE 7/0.2	0	M	140 MM
029	LS/017148/00 PVC 7/0.2 VIO/YELL 61-12PT T1	0	M	140 MM
030	LS/016820/00 WIRE PVC 7/0.2 RED/ORANGE	0	M	140 MM

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
T01				0		THIS PL ASSY TO B86882
001	AS/002636/00	CONN MINI LATCH 26 WAY	BERG	1	EA	SKT 27
002	AS/002624/00	CONN (CHAMP) RP 2-552273-1 AMP		1	EA	SKT 40
003	AS/002251/00	MINI P.V. CONTACTS 47565		25	EA	
004	SS/024477/00	PAINT AIR DRYING WH 22 HUMBRØL		0	LT	A/R
005	LS/017071/00	TY-RAP TYPE TY-51M		2	EA	
006	LS/016504/00	WIRE 7/0.2 6-12-PT6-T1 BLACK		0	M	140 MM
007	LS/016549/00	WIRE 7/0.2 6-12-PT6-T1 BROWN		0	M	140 MM
008	LS/016548/00	WIRE 7/0.2 6-12-PT6-T1 RED		0	M	140 MM
009	LS/016546/00	WIRE 7/0.2 6-12-PT6-T1 ORANGE		0	M	140 MM
010	LS/016506/00	WIRE 7/0.2 6-12-PT6-T1 GREEN		0	M	140 MM
011	LS/016505/00	PVC WIRE 7/0.2 61-12-PT6-T1 BU		0	M	140 MM
012	LS/016545/00	PVC WIRE 7/0.2 61-12-PT6-T1 SL		0	M	140 MM
013	LS/016560/00	PVC 7/0.2 YELLOW TYPE 1.		0	M	140 MM
014	LS/016561/00	WIRE 7/0.2 6-12-PT6-T1 WHITE		0	M	140 MM
015	LS/016871/00	WIRE 7X0.2 PVC TYPE 1 GREY/BRN		0	M	140 MM
016	LS/016873/00	WIRE 7X0.2 PVC TYPE 1 GRY/GRGE		0	M	140 MM
017	LS/016874/00	WIRE 7X0.2 PVC TYPE 1 GREY/GRN		0	M	140 MM
018	LS/016875/00	WIRE 7X0.2 PVC TYPE 1 GREY/BL		0	M	140 MM
020	LS/016878/00	WIRE 7X0.2 PVC TYPE 1 WHT/RED		0	M	140 MM
021	LS/016879/00	WIRE 7X0.2 PVC TYPE 1 WHT/GRG		0	M	140 MM
022	LS/016880/00	WIRE 7X0.2 PVC TYPE 1 WHT/GRN		0	M	140 MM
023	LS/016881/00	WIRE 7X0.2 PVC TYPE 1 WHE/BLUE		0	M	140 MM
024	LS/016827/00	WIRE 7/0.2 61-12-PT6-T1 WH/SL		0	M	140 MM
025	LS/016860/00	WIRE 7X0.2 PVC TYPE 1 RED/BLUE		0	M	140 MM

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
026	LS/016819/00 PVC WIRE RED/BROWN SIZE 7/02	0	M	140 MM
027	LS/017275/00 PVC WIRE INS 7/0.2 BLK/BROWN	0	M	140 MM
028	LS/016825/00 BLACK ORANGE 7/0.2	0	M	140 MM
029	LS/017148/00 PVC 7/0.2 VIO/YELL 61-12PT T1	0	M	140 MM
030	LS/016820/00 WIRE PVC 7/0.2 RED/ORANGE	0	M	140 MM
032	AS/002710/00 STRAIN RELIEF CLAMP 1-552298-1	1	EA	

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
T01				0		ASSY DRG- B86885
001 AS/002625/00	CONN MINI LATCH 65043-031	BERG	1		EA	SKT 25
002 AS/001650/00	SOCKET 25 WAY DB25S CANNON		1		EA	SKT 39
003 AS/002251/00	MINI P.V. CONTACTS 47565		12		EA	
004 SS/024477/00	PAINT AIR DRYING WH 22 HUMBRÖL		0		LT	A/R
005 LS/017071/00	TY-RAP TYPE TY-51M		2		EA	
006 LS/016504/00	WIRE 7/0.2 6-12-PT6-T1 BLACK		0		M	560 MM
007 LS/016548/00	WIRE 7/0.2 6-12-PT6-T1 RED		0		M	560 MM
008 LS/016546/00	WIRE 7/0.2 6-12-PT6-T1 ORANGE		0		M	280 MM
009 LS/016545/00	PVC WIRE 7/0.2 61-12-PT6-T1 SL		0		M	280 MM
010 LS/016561/00	WIRE 7/0.2 6-12-PT6-T1 WHITE		0		M	560 MM
011 LS/016858/00	WIRE 7X0.2 PVC TYPE 1 RED/BLK		0		M	560 MM
012 LS/016876/00	WIRE 7X0.2 PVC TYPE 1 WHT/BLK		0		M	560 MM

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
001	PL/090881/00	# TEST FILTER BOX ASSY		1	EA	TEST FILTER BOX
002	086727/00	1 B PLASTIC BAG		1	EA	
004	AS/002645/00	1 PLUG 3 POLE S104A040 SEAELECTRØ		2	EA	
005	AS/002646/00	1 PLUG 4 POLE S104A037 SEAELECTRØ		1	EA	
006	AS/002647/00	1 PLG 4MM 1 POLE 10A Y20724/GN		3	EA	
007	AS/002648/00	1 PLG 4MM 1 POLE 10A Y20724/RED		3	EA	
008	AS/002649/00	1 PLG 4MM 1 POLE 10A Y20724/BK		3	EA	
009	MS/050093/00	1 INSTRUCTION MANUAL FOR SE 2450		1	EA	
010	RS/023150/00	1 FUSE LINK 2A L2080 BELLING LEE		1	EA	FS1 (230V)
011	RS/023304/00	1 FUSE LINK 4A 19195/4A LITTLE		1	EA	FS1 (115V)
012	RS/023305/00	1 FUSE LINK 2.5A L2080A/2,5A B&L		1	EA	FS11
013	RS/023023/00	1 CARTRIDGE FUSE 15A L 1055 BELL		1	EA	FS13
014	RS/023304/00	1 FUSE LINK 4A 19195/4A LITTLE		1	EA	FS12

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
001	PL/090881/00	# TEST FILTER BOX ASSY		1	EA	TEST FILTER BOX
002	086727/00	1 B PLASTIC BAG		1	EA	
004	AS/002645/00	1 PLUG 3 PØLE S104A040 SEALECTRØ		2	EA	
005	AS/002646/00	1 PLUG 4 PØLE S104A037 SEALECTRØ		1	EA	
006	AS/002647/00	1 PLG 4MM 1 PØLE 10A Y20724/GN		3	EA	
007	AS/002648/00	1 PLG 4MM 1 PØLE 10A Y20724/RED		3	EA	
008	AS/002649/00	1 PLG 4MM 1 PØLE 10A Y20724/BK		3	EA	
009	MS/050093/00	1 INSTRUCTION MANUAL FØR SE 2450		1	EA	
010	RS/023150/00	1 FUSE LINK 2A L2080 BELLING LEE		1	EA	FS1 (230V)
011	RS/023304/00	1 FUSE LINK 4A 19195/4A LITTLE		1	EA	FS1 (115V)
012	RS/023305/00	1 FUSE LINK 2.5A L2080A/2,5A B&L		1	EA	FS11
013	RS/023023/00	1 CARTRIDGE FUSE 15A L 1055 BELL		1	EA	FS13
014	RS/023304/00	1 FUSE LINK 4A 19195/4A LITTLE		1	EA	FS12

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
001	086872/01	4	D ASSY PRG	0	EA	REF ONLY
002	092370/00	4	D COT DIAG	0	EA	REF ONLY
005	086875/01	1	A MONITOR MODULE KIT	1	EA	
006	DS/033997/00	1	RES 12 OHM .25W 5% CR25	1	EA	R1
007	DS/034870/00	1	RES 75R 1% 0.4W 100PPM MR25	2	EA	R2,10
008	DS/036439/00	1	RES 330R 10% 1/2W	1	EA	R4
009	DS/036408/00	1	RES 22K 10% 1/2W EB A BRADLEY	2	EA	R5,6
010	DS/036404/00	1	RES 1K5 10% 1/2W EB A BRADLEY	1	EA	R7
011	DS/033943/00	1	R 470R 5% 1/4W CR25 MULLARD	1	EA	R8
012	DS/033962/00	1	R 1M 5% 1/4W CR25 MULLARD	1	EA	R11
013	US/033964/00	1	R 1M8 10% 1/4W CR25 MULLARD	1	EA	R12
014	DS/034037/00	1	R 27K 5% 1/4W CR25 MULLARD	1	EA	R13
015	DS/034001/00	1	R 27R 5% 1/4W CR25 MULLARD	1	EA	R14
016	DS/034051/00	1	R 390K 5% 1/4W CR25 MULLARD	1	EA	R15
017	DS/033954/00	1	R 22K 5% 1/4W CR25 MULLARD	1	EA	R16
018	DS/036335/00	1	RES 390R 5% 1.6W PR37-390R MUL	1	EA	R17
019	DS/033956/00	1	R 82K 5% 1/4W CR25 MULLARD	1	EA	R18
020	DS/033942/00	1	R 330R 5% 1/4W CR25 MULLARD	1	EA	R19
021	DS/033951/00	1	R 10K 5% 1/4W CR25 MULLARD	1	EA	R20
022	FS/C10901/00	1	POT 100K 20% 1/2W	2	EA	RV2,4
028	FS/010899/00	1	POT 470K 25% 1/2W	1	EA	RV3
029	FS/010251/00	1	POT 1M MP DEALER PLESSEY	1	EA	RV5
030	FS/010595/00	1	POT 1K CMP/PC PLESSEY	1	EA	RV6
031	FS/010779/00	1	POT 47K 20% 90H	1	EA	RV7
036	BS/005334/00	1	DIODE BA159 I.T.T	4	EA	D1,3,5,6

IT COMP. NUMBER S STOCK DESCRIPTION QTY UN NOTES

074	LS/017537/00	1	TY-RAP.	TY-23M. T.BETTS	6	M	
075	0S/021153/00	1	SLEEVING RIFILEG	GY 6/10 ALCR	0	FT	0,53M LG
076	SS/024607/00	1	LAQUER AEROSOL	CLEAR CPL-397	0	EA	A/R
079	LS/016017/00	1	WIRE.5KG RL	22SWG	0	KG	0.2M
081	LS/016886/00	1	WIRE 16/0.2	TYPE 2 PVC ORANGE	0	M	0,2M LG
082	LS/016889/00	1	W WIRE 16/0.2	PVC TYPE 2 BLUE	0	M	0,45M LG
083	LS/016888/00	1	W WIRE 16/0.2	61-12 PT6 T2 GM	0	M	0,2M LG
084	LS/016887/00	1	W WIRE 16/0.2	61-12 PT6 T2 YL	0	M	0,35M LG
085	LS/016890/00	1	WIRE 16/0.2	TYPE 2 VIOLT	0	M	0,3M LG
086	LS/016916/00	1	WIRE 16/0.2	TYPE 2 WHIT/ORG	0	M	0,25M LG
087	LS/016883/00	1	WIRE 16/0.2	TYPE 2 PVC BLACK	0	M	0,15M LG
090	LS/017580/00	1	WIRE BLK./ORAN.	16/02 PVC TYPE	0	M	0,25M LG
091	LS/017578/00	1	WIRE BLUE/BRN.	16/02 PVC TYPE 2	0	M	0,25M LG
092	LS/017579/00	1	WIRE BLUE/ORAN.	16/02 PVC TYPE	0	M	0,25M LG

IT COMP.	NUMBER	S STOCK	DESCRIPTION	QTY	UM	NOTES
T01	081221/01	4	E ASSY DRG SHTS 1 & 2 (SE2450)	0	EA	REF.ONLY
T02	092106/00	4	E COT DIAG (SE2450)	0	EA	REF.ONLY
005	PL/082071/01	5	PCB ASSY,POWER SPLY 111 SE2450	1	EA	
006	PL/082076/01	5	PCB ASSY,POWER SPLY 211 SE2450	1	EA	
007	PL/082081/01	5	PCB ASSY,PSU MOTHERBRD 1SE2450	1	EA	
008	PL/091121/01	5	TOR.TRANS.C/FORM ASSY (SE2450)	1	EA	
009	PL/091122/01	5	P.S.C/FORM NO.1 ASSY (SE2450)	1	EA	
010	092945/00	1	B RETAINING PLATE	2	EA	
011	PL/092463/00	#	SW & FUSE LABEL ASSY (SE2450)	1	EA	
012	PL/086841/00	1	BOTTOM BRACKET ASSY SE2450	1	EA	
013	PL/086844/01	#	TOP BRACKET ASSY (SE2450)	1	EA	
014	PL/086986/01	#	END PLATE SCREENED	1	EA	
015	PL/088962/00	5	EARTH LINK ASSY SE2450	1	EA	
016	092467/00	1	E BACK PANEL CASTING (SE2450)	1	EA	
017	086845/00	1	C BOTTOM PLATE	1	EA	
018	092946/00	1	C COVER 2450	1	EA	
019	086856/00	1	A SPACER,SHORT,HEX	2	EA	
020	086857/00	1	A SPACER,LONG,HEX	2	EA	
021	086859/00	1	A SPACER,PCB	1	EA	
022	045303/00	1	C LIGHTNING FLASH	1	EA	
023	082666/00	1	A POWER INPUT LABEL	1	EA	
030	RS/023040/00	1	FUSE HOLDER FOR SIZE 1 L1302/B	1	EA	FOR FS 13
031	RS/023042/00	1	FUSE HOLDER LID L1303L BEL-LEE	1	EA	FOR ITEM 30
032	S/023148/00	1	FUSE HOLDER E6011 BELLING LEE	3	EA	FOR FS1,11,12
033	RS/023304/00	1	FUSE LINK 4A 19195/4A LITTLE	1	EA	FS12

IT COMP. NUMBER S STOCK DESCRIPTION										QTY	UN	NOTES
076	YS/040107/00	1	SC P0Z	PAN M5 X 16		MSZP	1		EA			
077	YS/040895/00	1	SCREW P0Z	PAN M4 X 55LG ST 28P			1		EA			
078	YS/040845/00	1	SC P0Z	PAN M4 X 50		MSZP	3		EA			
079	YS/040098/00	1	SC P0Z	PAN M4 X 16		MSZP	2		EA			
080	YS/040096/00	1	SC P0Z	PAN M4 X 10		MSZP	1		EA			
081	YS/040095/00	1	SC P0Z	PAN M4 X 8		MSZP	4		EA			
082	YS/040014/00	1	SC P0Z	CSK M4 X 16		MSZP	1		EA			
083	YS/040090/00	1	SC P0Z	PAN M3 X 16		MSZP	6		EA			
084	YS/040086/00	1	SC P0Z	PAN M3 X 6		MSZP	12		EA			
085	YS/040680/00	1	SC P0Z	PAN M3 4	MSZP		6		EA			
086	YS/040005/00	1	SC P0Z	CSK M3 X 12		MSZP	2		EA			
087	YS/040006/00	1	SC P0Z	CSK M3 X 16		MSZP	2		EA			
088	YS/040367/00	1	NUT HEX	FULL M5		MSZF	2		EA			
089	YS/040386/00	1	NUT HEX	FULL M4		MSZP	4		EA			
090	YS/040385/00	1	NUT HEX	FULL M3		MSZP	8		EA			
091	YS/040402/00	1	WASHER STD	M4 HEAVY		MSZP	3		EA			
092	YS/040401/00	1	WASHER STD	M3 HEAVY		MSZP	14		EA			
093	YS/040462/00	1	WASHER CRINKLE	M4		BCUCP	3		EA			
094	YS/040461/00	1	WASHER CRINKLE	M3		BCUCP	27		EA			
095	YS/040435/00	1	WASHER SHK/PRF	M5 INT/T		MSCP	1		EA			
096	YS/040434/00	1	WASHER SHK/PRF	M4 INT/T		MSCP	14		EA			
097	YS/040433/00	1	WASHER SHK/PRF	M3 INT/T		MSCP	6		EA			
098	YS/040002/00	1	SC P0Z	CSK M3 X 6		MSZP	4		EA			
099	YS/040281/00	1	SC P0Z	TAPCSK M3 X 6		MSZP	4		EA			
100	SS/024401/00	1	FOAM RUBBER	ADH TAPE7X4MM	TES		0		RL			50MM LG

PARTS LIST 081221/01 ISSUE 02 C.N. 10140 DATE 14/05/82 C>POWER SUPPLY 1 ASSY SE2450 0000000000

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
105	LS/017206/00 1 WIRE PVC 24/02 BRN 61-12 PT6T2	0	M	100MM LG
106	LS/017306/00 1 PVC WIRE 24.02 WHT/BLK P6 T2	0	M	100MM LG
107	LS/016950/00 1 WIRE PVC 32/0,2 TYPE3 BK	0	M	300MM LG
110	05/021330/00 1 TUBING PVC 4MM I/D BK XY40 HEL	0	M	130MM LG
111	05/020613/00 1 SLEEVE 3X20 PINK H/MAW H3C	7	EA	
114	LS/017537/00 1 TY-RAP. TY-23M. T.BETTS	3	EA	

IT COMP. NUMBER S STOCK DESCRIPTION				QTY	UN	NOTES
T01	082081/01	A D ASSY DRG	(SE2450)	0	EA	REF. ONLY
T02	092106/00	A E COT DIAG	(SE2450)	0	EA	REF. ONLY
D03	092491/00	A MOD RECORD SHEET	(SE2450)	0	EA	REF ONLY
D04	092492/00	A ASSY STATE SHEET	(SE2450)	0	EA	REF ONLY
D06	092888/00	A INSULATOR		1	EA	
D07	PL/092482/00	PCB DRILLED,PS 1,M.BOARD	2450	1	EA	
D09	DS/034911/00	RES 121K 1% 0.4W 50PPM	MR25VTM	1	EA	R70
D10	DS/034095/00	R 10K 1% 0.4W 50PPM	MR25/VTM	2	EA	R68,69
D11	DS/034877/00	RES 221R 1% 0.4W 100PPM	MR25	1	EA	R8
D14	CS/032736/00	CAP 0.22 MF 10% 100V	8131-M100	1	EA	C10
D15	CS/032729/00	CAP 2200MF 25V 2222-106-36223		1	EA	C31
D16	CS/031280/00	CAP 1500MF +50-10% 017-15152		1	EA	C9
D17	CS/032725/00	CAP 22MF 20% 25V TAG 62/25 1TT		1	EA	C44
D18	CS/032733/00	CAP 10,000 MF +50-10% 25V	ERIE	1	EA	C29
D19	CS/033093/00	CAP 0,22MF 20% 50V CERAM,RDL		1	EA	C48
D21	BS/005701/00	2.DIODE 6V2 5W IM5341 B	MOTRA	1	EA	D9
D22	BS/006240/00	CIRCUIT PROTECTOR	CGB-16-6.2	1	EA	D29
D23	BS/005734/00	BRIDGE RECT 1.2A 400V	1KAB40	1	EA	D8
D24	BS/005710/00	IC LM340T-50	NATIONAL ONLY	1	EA	REG 2
D25	BS/005769/00	I.C 1LQ 74	LITRONIX ONLY	1	EA	IC1
D26	BS/005661/00	TRANSISTOR,SIGNAL	BC184 (CC)	2	EA	TR9,14
D29	HS/012251/00	RELAY 2 POLE C/O PRME	2A-005B	1	EA	RLA
D32	AS/002572/00	CONN 58WAY 2-87215	AMP	1	EA	PL8
D33	AS/002580/00	CONN 2X18 WAY	PCGD-18K-17GE00	2	EA	SKT6,7
D34	AS/002834/00	SKT 20WAY	MHD20DM0101ML/M31182	0	EA	* ALTN TO ITEM 33

IT COMP. NUMBER S STOCK DESCRIPTION QTY UN NOTES

035	BS/002420/00	1	MOUNTING PAD 10171 M.ROSS	2	EA	FOR TR9,14
036	BS/005356/00	1	HEATSINK 104 REDPOINT	1	EA	FOR REG 2
037	MS/019719/00	1	CAP CLIP DT2254 MULLARD	1	EA	FOR C31
038	MS/019063/00	1	CLIP CAPACITOR TYPE V3/32104/6	1	EA	FOR C29
039	OS/020220/00	1	LACING CARD NYLON,BLACK R88W	0	RL	100MM FOR C9
040	KS/015007/00	1	TERMINAL LUG H20722 HARWIN	1	EA	
042	YS/040088/00	1	SC P0Z PAN M3 X 10	MSZP 1	EA	
043	YS/040089/00	1	SC P0Z PAN M3 X 12	MSZP 2	EA	
044	YS/040090/00	1	SC P0Z PAN M3 X 16	MSZP 1	EA	
045	YS/040097/00	1	SC P0Z PAN M4 X 12	MSZP 2	EA	
046	YS/040098/00	1	SC P0Z PAN M4 X 16	MSZP 1	EA	
047	YS/040401/00	1	WASHER STD M3 HEAVY	MSZP 4	EA	
048	YS/040407/00	1	WASHER LARGE M4 HEAVY	MSZP 3	EA	
049	YS/040461/00	1	WASHER CRINKLE M3	BCUCP 4	EA	
050	YS/040462/00	1	WASHER CRINKLE M4	BCUCP 3	EA	
051	YS/040385/00	1	NUT HFX FULL M3	MSZP 4	EA	
052	YS/040386/00	1	NUT HEX FULL M4	MSZP 3	EA	
053	YS/040404/00	1	WASHER STD M6 HEAVY	MSZP 1	EA	
054	LS/017199/00	1	WRE 63/02 BK 61-12 PT6 T3	0	M	200MM LG
055	SS/024248/00	1	HEATSINK COMPOUND DP2623	0	EA	A/R
056	KC/015747/00	1	SOLDER TAG 2BA 204 ROSS-COURT	1	EA	
057	YS/040436/00	1	WASHER SHK/PRF M6 INT/T MSCP	1	EA	
058	YS/041566/00			2		

IT COMP.	NUMBER	S	STOCK DESCRIPTION	QTY	UN	NOTES
T01	082071/01	4	D ASSY DRG	0	EA	REF.ONLY
			(SEE2450)			
T02	092106/00	4	E COT DIAG	0	EA	REF.ONLY
			(SEE2450)			
003	092433/00	4	A MOD STATE SHEET	0	EA	REF ONLY
			(SEE2450)			
004	092434/00	4	A ASSY STATE SHEET	0	EA	REF ONLY
			(SEE2450)			
005	PL/092436/00	1	PCB DRILLED,PS NO 1,T1	1	EA	
			2450			
012	DS/036332/00	1	RES 1R2 10% 2.5W W21	2	EA	R6,11
			MELWYN			
013	DS/036333/00	1	RES 1R2 10% 2.5W 74EV	0	EA	* ALTN TO ITEM 12
			ERG			
014	DS/034760/00	1	2R7 5% 2.5W W21	2	EA	R2,9
			MELWYN			
015	DS/035833/00	1	R 12K4 1% 0.4W 50PPM MR25/VTM	2	EA	R73,75
016	DS/034877/00	1	RES 221R 1% 0.4W 100PPM MR25	2	EA	R1,15
017	DS/035786/00	1	R 4K02 1% 0.4W 50PPM MR25/VTM	4	EA	R3,7,10,14
018	DS/034892/00	1	RES 2K 1% 0.4W 100PPM MR25	2	EA	R4,12
019	DS/034099/00	1	R 30K1 1% 0.4W 50PPM MR25/VTM	2	EA	R5,13
020	DS/034893/00	1	RES 2K43 1% 0.4W 100PPM MR25	2	EA	R72,74
027	CS/030264/00	1	CAP 47PF 5% 160V HS SUPLEX	2	EA	C7,15
028	CS/031596/00	1	CAP 0.22MFD 10% 100V 344-21224	2	EA	C2,18
029	CS/032840/00	1	CAP 4.7MF 50V 20% TAP 4.7/50	4	EA	C5,8,13,16
030	CS/032859/00	1	CAP 470MF -10<50% 63V EN12 11T	4	EA	C3,6,11,14
031	CS/031280/00	1	CAP 1500MF +50-10% 017-15152	2	EA	C1,17
032	CS/033093/00	1	CAP 0.22MF 20% 50V CERAM.RDL	?	EA	C47,49
040	BS/005701/00	1	Z.DIODE 6V2 5W IN5341 B MOTRA	2	EA	D2,16
042	BS/003561/00	1	LED T1L209 T1 SUPPLY	7	EA	D3,5,7,10,12,14,17
044	BS/005734/00	1	BRIDGE RECT 1.2A 400V 1KAB40	6	EA	D1,4,6,11,13,15
046	BS/002795/00	1	TRANSISTOR 2N4919 MOTOROLA	4	EA	TR1-4
048	BS/005710/00	1	IC LM340T-50 NATIONAL ONLY	2	EA	REG 1,3

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
050 BS/005706/00	1 IC LM104H NATIONAL ONLY	2	EA	REG 4,6
052 BS/005707/00	1 IC LM105H NATIONAL ONLY	2	EA	REG 5,7
061 FS/010833/00	1 POT 5K 10% 0.5W 85X-5K BRADLEY	4	EA	RV1-4
064 RS/023303/00	1 FUSE 1A TIME DELAY 5X20 19195	1	EA	FS8
065 RS/0233324/00	1 FUSE 250MA TYPE T GLASS MULTI	4	EA	FS3,4,6,7
066 RS/0233326/00	1 FUSE 500MA TYPE T GLASS MULTI	2	EA	FS2,5
067 RS/023133/00	1 FUSEHOLDER L1426	7	EA	FOR MTG ITEM 65 & 66
071 BS/005356/00	1 HEATSINK TV4 REDPOINT	2	EA	FOR MTG REG 1,3
073 BS/005597/00	1 HEATSINK T0220 TV1500 REDPOINT	4	EA	FOR MTG TR1-4
075 BS/002343/00	1 HEAT SINK SF2 REDPOINT	4	EA	FOR MTG REG 4-7
076 BS/003172/00	1 I/C MOUNTING PAD MON 8L JERMYN	2	EA	FOR MTG REG 5,7
077 BS/003135/00	1 DIODE HOLDER A1136 JERMYN	2	EA	FOR MTG C7 & 15
078 BS/005061/00	1 TRANSISTOR MTG PAD MON10/LF	2	EA	FOR MTG REG 4,6
079 SS/024248/00	1 HEATSINK COMPOUND DP2623	0	EA	A/R FOR MTG TR1-4, REG 1,3
080 AS/002575/00	1 CONN 6 WAY A2391 09-72-1061 MX	1	EA	PL2
082 AS/002577/00	1 CONN 8 WAY A.2391 09-72-1081	1	EA	PL1
084 MS/028003/00	1 BEADS CERAMIC N02	8	EA	FOR MTG R2,6,9,11
087 YS/040088/00	1 SC P02 PAN M3 X 10 MSZP	6	EA	
096 YS/040461/00	1 WASHER CRINKLE M3 BCUCP	6	EA	
100 YS/040385/00	1 NUT HEX FULL M3 MSZP	6	EA	
102 OS/020220/00	1 LACING CARD NYLON, BLACK R88W	0	RL	0,3M LG

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
T01	082076/01 4 D ASSY DRG (SEE2450)	0	EA	REF ONLY
T02	092106/00 4 E CCT DIAG (SEE2450)	0	EA	REF ONLY
003	092107/00 4 A ASSY STATE SHEET (SEE2450)	0	EA	REF ONLY
004	092108/00 4 A MOD RECORD SHEET	0	EA	REF ONLY
005	PL/092111/00 1 PCB DRILLED P.S.NO.2 T.1, 2450	1	EA	
010	DS/0344872/00 1 R 100R 1% 0.4W 50PPM MR25/VTM	3	EA	R45,71,76
011	DS/033525/00 1 RES 200 OHMS 1% 0.4W MR25	1	EA	R46
012	DS/034093/00 1 R 5K62 1% 0.4W 50PPM MR25/VTM	2	EA	R41,51
013	DS/034410/00 1 R 3K92 1% 0.4W 50PPM MR25/VTM	1	EA	R50
014	DS/034900/00 1 R 27K4 1% 0.4W 50PPM MR25/VTM	1	EA	R48
015	DS/0344219/00 1 R 18K2 1% 0.4W 50PPM MR25/VTM	2	EA	R49,34
016	DS/034095/00 1 R 10K 1% 0.4W 50PPM MR25/VTM	4	EA	R57,58,59,60,
017	DS/033756/00 1 RES 1K2 2% 0.4W 100PPM MR25	1	EA	R52
018	DS/034430/00 1 R 909R 1% 0.4W 50PPM MR25/VTM	2	EA	R18,56
019	DS/033876/00 1 R 1K 1% 0.4W 50PPM MR25/VTM	2	EA	R55,62
020	DS/034887/00 1 R 1K1 1% 0.4W 50PPM MR25/VTM	1	EA	R53
021	DS/034881/00 1 RESISTOR 392 OHM 1% 0.4W MR25	1	EA	R54
022	DS/034877/00 1 RES 221R 1% 0.4W 100PPM MR25	1	EA	R61
023	DS/034897/00 1 R 4K75 1% 0.4W 50PPM MR25/VTM	1	EA	R63
024	DS/034865/00 1 RES 47R5 1% 0.4W 50PPM MR25	1	EA	R64
027	DS/033765/00 1 RES 3K0 2% 0.4W 100PPM MR25	1	EA	R42
028	DS/034884/00 1 R 511R 1% 0.4W 50PPM MR25/VTM	2	EA	R37,44
029	DS/033763/00 1 RES 2K4 2% 0.4W 100PPM MR25 ML	2	EA	R26,30
030	DS/034858/00 1 RES 24.3R 1% 0.4W 100PPM MR25	1	EA	R32
031	DS/033539/00 1 R 5K11 1% 0.4W 50PPM MR25/VTM	1	EA	R31

IT COMP. NUMBER S STOCK DESCRIPTION

QTY

UN

NOTES

032 DS/034849/00 1 R 10R0 1% 0.4W 50PPM MR25/VTM 2 EA R16,33

033 DS/034060/00 1 RES 12K1 1% .4W MR25 VTM/471 1 EA R36

034 DS/034891/00 1 RES 1K62 1% 0.4W 100PPM MR25 1 EA R22

035 DS/035833/00 1 R 12K4 1% 0.4W 50PPM MR25/VTM 1 EA R28

036 DS/035854/00 1 R 20K5 1% 0.4W 50PPM MR25/VTM 1 EA R19

037 DS/034869/00 1 RES 68.1R 1% 0.4W 100PPM MR25 1 EA R17

038 DS/035786/00 1 R 4K02 1% 0.4W 50PPM MR25/VTM 2 EA R21,27

039 DS/034892/00 1 RES 2K 1% 0.4W 100PPM MR25 2 EA R25,43

040 DS/034871/00 1 RES 90.9R 1% 0.4W 100PPM MR25 1 EA R23

041 DS/034099/00 1 R 30K1 1% 0.4W 50PPM MR25/VTM 1 EA R29

042 DS/036381/00 1 RES 0R1 10% 6W 58EV ERG 2 EA R65,67

043 DS/034760/00 1 2R7 5% 2.5W W21 MELWYM 2 EA R20,24

044 DS/035744/00 1 R 1K47 1% 0.4W 50PPM MR25/VTM 1 EA R77

045 DS/034639/00 1 0R30 10% 2.5W W21 2 EA R35,40

046 DS/034880/00 1 RES 365R 1% 0.4W 100PPM MR25 1 EA R38

047 DS/034861/00 1 RES 33.2R 1% 0.4W 100PPM MR25 1 EA R39

049 FS/010909/00 1 POT TRIM 1K 10% 0.5W 85X/1K 1 EA RV8

050 FS/010832/00 1 POT 2K 10% 0.5W 85X-2K BRADLEY 1 EA RV9

051 FS/010833/00 1 POT 5K 10% 0.5W 85X-5K BRADLEY 3 EA RV5,6,10

052 FS/010592/00 1 POT 2.2K0HMS CERMET CMP/PC 1 EA RV7

056 CS/031814/00 1 CAP 820PF 2.5% 30V HS SUFLEX 1 EA C46

057 CS/032076/00 1 CAP 68PF 2.5% 63V HS SUFLEX 1 EA C23

058 CS/031739/00 1 CAP 1000 PF 21/2% 30V HS30 1 EA C20

059 CS/004135/00 1 CAP 2200PF 10% 160V HS SUFLEX 1 EA C26

060 CS/031723/00 1 CAP 0.1MFD 10% 100V 8131M100 1 EA C27

IT COMP. NUMBER	S STOCK DESCRIPTION	QTY	UN	NOTES
061	CS/031313/00 1 CAP 330MF +50710X 017-18331	2	EA	C19,22
062	CS/032726/00 1 CAP 10MF 20X 50V TAP 10/50 1TT	2	EA	C21,24
063	CS/031042/00 1 CAP 4.7MF 20X 35V TAB 1TT	2	EA	C37,40
064	CS/032663/00 1 CAP 22MFD 20X 35V TAP22-35	2	EA	C28,30
066	CS/031271/00 1 CAP 2200MF +50710X 017-14222	1	EA	C33
067	CS/032949/00 1 CAP 0.01MF -20+80X 50V (CC)	1	EA	C50
070	BS/003561/00 1 LED T1L209 T1 SUPPLY	5	EA	D19,21,24,26,28
072	BS/005734/00 1 BRIDGE RECT 1.2A 400V 1KAB40	2	EA	D18,20
076	BS/002795/00 1 TRANSISTOR 2N4919 MOTOROLA	2	EA	TR5,7
077	BS/003194/00 1 TRANSISTOR 2N2905A TEXAS	2	EA	TR6,11
078	BS/005213/00 1 TRANSISTOR 2N2222 TEXAS	1	EA	TR13
079	BS/002838/00 1 TRANSISTOR MPS3640 MOTOROLA	1	EA	TR8
080	BS/006192/00 1 TRANSISTOR TL430C TEXAS ONLY	1	EA	TR9
084	BS/005706/00 1 IC LM104H NATIONAL ONLY	1	EA	REG 8
085	BS/005707/00 1 IC LM105H NATIONAL ONLY	1	EA	REG 9
086	BS/005708/00 1 IC LM304H NATIONAL ONLY	1	EA	REG 10
087	BS/005971/00 1 I.C. MC1723C6 MOTOROLA ONLY	1	EA	REG 11
088	BS/003526/00 1 I.C. LM 741CN MAT SEM ONL	1	EA	IC2
089	BS/006193/00 1 I.C. TL494CN TEXAS ONLY	1	EA	REG 12
093	ES/008655/00 1 COIL 50UH A92371	1	EA	L1
095	RS/023326/00 1 FUSE 500MA TYPE T GLASS MULTI	2	EA	FS9,10
096	RS/023133/00 1 FUSEHOLDER L1426	2	EA	FOR ITEM 95
098	AS/002576/00 1 CONN 4 WAY A-2391 09-72-1041	1	EA	PL3
099	AS/002575/00 1 CONN 6 WAY A2391 09-72-1061 MX	1	EA	PL5
100	AS/002577/00 1 CONN 8 WAY A.2391 09-72-1081	1	EA	PL4

PARTS LIST 082076/01 ISSUE 03 C.N. 10223 DATE 04/11/82 C>POWER SUPPLY PCB NO 2 ASSY TYPE 1 SE2450 00000000000

IT COMP. NUMBER S STOCK DESCRIPTION QTY UN NOTES

102	BS/002420/00	1	MOUNTING PAD 10171 M.ROSS	2	EA	FOR MTG TR8,9
103	BS/002968/00	1	MOUNTING PAD T05/18/002 JERMYN	1	EA	FOR MTG TR13
104	BS/002747/00	1	TRANSISTOR PAD T05-001	2	EA	FOR MTG TR6,11
105	BS/003172/00	1	I/C MOUNTING PAD M0N 8L JERMYN	1	EA	FOR MTG REG.9
106	BS/005061/00	1	TRANSISTOR MTG PAD M0M10/LF	3	EA	FOR MTG REG.8,10,11
107	BS/003135/00	1	DIODE HOLDER A1136 JERMYN	4	EA	FOR MTG C20,23,26,46
108	WS/028003/00	1	BEADS CERAMIC M02	8	EA	FOR MTG R20,24,35,40
109	KS/015007/00	1	TERMINAL LUG H20722 HARWIN	6	EA	FOR MTG L1,R65,67
110	BS/005705/00	1	HEATSINK TV21 REDPOINT	2	EA	FOR TR5,7
111	BS/002343/00	1	HEAT SINK SF2 REDPOINT	4	EA	FOR REG.8,9,10,11
112	SS/024248/00	1	HEATSINK COMPOUND DP2623	0	EA	A/R FOR USE WITH ITEM 110
114	OS/020220/00	1	LACING CARD NYLON,BLACK R88W	0	RL	0.15M FOR SECURING C19,22,33
116	YS/040088/00	1	SC P02 PAM M3 X 10 MSZP	4	EA	FOR SECURING TR5,7
117	YS/040461/00	1	WASHER CRINKLE M3 BCUCP	4	EA	FOR SECURING TR5,7
118	YS/040385/00	1	MUT HEX FULL M3 MSZP	4	EA	FOR SECURING TR5,7
119	YS/040096/00	1	SC P02 PAM M4 X 10 MSZP	1	EA	FOR SECURING L1
120	YS/040462/00	1	WASHER CRINKLE M4 BCUCP	1	EA	FOR SECURING L1
130	OS/021330/00	1	TUBING PVC 4MM I/D BK XY40 HEL	0	M	100MM FOR L1

MP MASTER



MA23378